Design and Simulation of a Flux-Locked-Loop for use in Low-Frequency Magnetometry Systems using DC SQUIDS

by

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Thesis presented in partial fulfilment of the requirements for the degree of Master of Engineering (Electronic) in the Faculty of Engineering at Stellenbosch University

Supervisor: Prof. C.J. Fourie

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Date: December 2021

Abstract

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This thesis presents the design of a Flux-Locked-Loop (FLL) for use in readout electronics for High Temperature Superconductor Superconducting Quantum Interference Devices (HTS SQUIDs). SQUIDs are used as extremely sensitive magnetometers in a wide range of fields, including biomedical measurements, geophysical exploration and space weather prediction. The low noise readout electronics used to control these magnetometers is prohibitively expensive and largely inaccessible to most researchers. As such, there is a need for the development of a low-cost control system that is suitable for the measurement of magnetic flux densities at extremely low frequencies. The proposed FLL consists of a low noise pre-amplifier, secondary amplifier with voltage offset removal, lock-in detector, integrator and feedback circuitry. In addition, it uses flux modulation and bias current reversal techniques to minimise the noise of the SQUID. The FLL configuration is designed to be flexible, with a microcontroller used to customise the circuit to the specifications of the SQUID. A number of pre-amplifier designs were evaluated to determine the most suitable implementation for this application. A full noise analysis of each design provides a useful evaluation tool for the suitability of the pre-amplifiers. The integrator and feedback system was designed to offer three sensitivity ranges, so that a wide range of magnetic flux measurements could be made. The proposed FLL design was simulated in LTspice XVII Circuit Simulator for a range of modelled magnetic flux inputs. The simulation results are very promising with the FLL accurately tracking the modelled magnetic flux input for a range of frequencies and magnetic flux densities. These simulation results suggest that, with a few improvements, the proposed FLL could be successfully implemented in a physical system. As a result, this thesis constitutes a promising step forward in reaching the goal of creating accessible low-cost SQUID readout electronics for low frequency magnetic flux density measurements.

Uittreksel

In hierdie tesis word die ontwerp van 'n vloedsluitlus (FLL) vir gebruik in uitleeselektronika vir Hoë-Temperatuur Supergeleier Kwantum-Inteferensie Toestelle (HTS SQUIDs) aangebied. SQUIDs word gebruik as uiters sensitiewe magnetometers op 'n wye verskeidenheid gebiede, insluitend biomediese metings, geofisiese verkenning en die meet en voorspelling van ruimteweer. Die gespesialiseerde laeruis uitleeselektronika wat gebruik word om hierdie magnetometers te beheer is baie duur en dus vir die meeste navorsers grootliks ontoeganklik. As sodanig is daar 'n behoefte aan die ontwikkeling van 'n goedkoop beheerstelsel wat geskik is vir die meting van magnetiese vloeddigthede by uiters lae frekwensies. Die voorgestelde FLL bestaan uit 'n laeruis-voorversterker, 'n sekondêre versterker wat die afsetspanning verwyder, 'n sluitdetektor, 'n integrator en 'n terugvoerstroombaan. Daarbenewens gebruik dit vloedmodulasie en voorspanningsomkeertegnieke om die ruis van die SQUID tot 'n minimum te beperk. Die buigsame FLL-opset gebruik 'n mikrobeheerder om die stroombaan aan te pas by die spesifikasies van die SQUID. 'n Aantal voorversterkerontwerpe is geëvalueer om die mees geskikte implementering vir hierdie toepassing te bepaal. 'n Volledige ruisontleding van elke ontwerp bied 'n nuttige evalueringsinstrument vir die geskiktheid van die voorversterkers. Die integrator en terugvoerstelsel is ontwerp om drie sensitiwiteitsreekse aan te bied, sodat 'n wye reeks magnetiese vloedmetings gedoen kan word. Die voorgestelde FLL-ontwerp is gesimuleer met die LTspice elektriese stroombaansimulator vir 'n reeks gemodelleerde magnetiese vloedintrees. Die simulasie-resultate is baie belowend, aangesien die FLL die gemodelleerde magnetiese vloedinvoer akkuraat volg vir 'n reeks frekwensies en magnetiese vloeddigthede. Hierdie simulasie-resultate dui daarop dat die voorgestelde FLL met 'n paar verbeterings suksesvol in 'n fisiese stelsel geïmplementeer kan word. As gevolg hiervan vorm hierdie tesis 'n belowende stap vorentoe om die doelwit te bereik om toeganklike goedkoop SQUID-uitleeselektronika vir laefrekwensie magnetiese vloeddigtheidmetings te skep.

Acknowledgements

Firstly, I would like to thank my supervisor Professor Coenrad J. Fourie, without whom this thesis would not have been possible. His guidance and support has been invaluable throughout. I would also like to thank Elda Saunderson from SANSA and Dr. Michal Janošek from the Czech Technical University in Prague for their advice and assistance with taking SQUID measurements for this thesis. I am extremely grateful to SANSA for funding my studies over the past two years. A special thanks to my mother and my sister, whose encouragement and support has motivated me throughout this process. Lastly, I would like to thank my family and friends for being there for me no matter what.

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Nomenclature

Constants

k	Boltzmann's constant	1.38×10^{-23} J/K
q	Charge on an electron	1.602×10^{-19} C
V_T	Thermal voltage	0.026 V at room temperature

Acronyms

AC	Alternating Current
BJT	Bipolar Junction Transistor
CMOS	Complementary Metal-Oxide-Semiconductor
DAC	Digital-to-Analog Converter
DAQ	Data Acquisition
DC	Direct Current
FLL	Flux-Locked-Loop
HTS	High Temperature Superconductor
IC	Integrated Circuit
ICSP	In-Circuit Serial Programming
JFET	Junction-gate Field-Effect Transistor
LNA	Low Noise Amplifier
LSB	Least Significant Bit
LTS	Low Temperature Superconductor
MISO	Master In Slave Out
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MOSI	Master Out Slave In
MSB	Most Significant Bit
PSRR	Power Supply Rejection Ratio
PWM	Pulse Width Modulation
RMS	Root Mean Square
SANSA	South African National Space Agency
SPDT	Single Pole Dual Throw
SPI	Serial Peripheral Interface
SPST	Single Pole Single Throw
SQUID	Superconducting Quantum Interference Device

Chapter 1

Introduction

1.1 Motivation

Superconducting Quantum Interference Devices (SQUIDs) are extremely sensitive magnetometers with applications in the fields of geophysical exploration, biomedical measurements, material sciences and microscopy [1]. Organisations such as the South African National Space Agency (SANSA) use SQUIDs to measure and predict space weather events [2]. For this particular application, the SQUIDs are required to measure magnetic flux densities with very low frequencies (< 1 Hz).

High Temperature Superconductor (HTS) SQUIDs can be immersed in liquid nitrogen, as opposed to Low Temperature Superconductor (LTS) SQUIDs, which have to be contained in liquid helium to operate correctly [1]. Liquid nitrogen is far cheaper and more accessible than liquid helium, and HTS SQUIDs are therefore preferred by research organisations such as SANSA.

To accurately measure magnetic flux densities with a HTS SQUID, readout electronics that use a Flux-Locked-Loop (FLL) is required. Currently, very few of these suitable readout electronics exist on the open market, with the available systems limited to pcSQUID™ from Star Cryoelectronics [3] and the SEL-1 from Magnicon [4]. These systems are prohibitively expensive and not available to most researchers with limited access to large amounts of funding.

1.2 Background

A magnetometer is defined as an "instrument for measuring the strength and sometimes the direction of magnetic fields, including those on or near the Earth and in space" [5]. A Superconducting Quantum Interference Device (SQUID) can function as an extremely sensitive magnetometer that operates using the principles of superconductivity.

Superconductivity is the phenomenon by which the electrical resistance of a conductor disappears below a specific temperature. This temperature is dependent on the material displaying superconducting properties. Some metals such as niobium require extremely low temperatures below 9.3 K to enter a superconducting state. Other compounds such as yttrium barium copper oxide (YBCO) are known as high temperature superconductors since they only require temperatures below 95 K [6].

One of the cornerstones of superconductivity is the Josephson effect. Theorised by physicist Brian D. Josephson in 1962, the Josephson effect describes how current would flow across a thin barrier placed between two superconductors due to the tunnelling of electrons across the barrier [7]. The device consisting of superconducting layers and a resistive barrier became known as a Josephson junction.

A DC SQUID consists of two Josephson junctions in a superconducting loop. The unique properties of this setup allow the SQUID to convert magnetic flux to voltage where magnetic flux is defined as "a measurement of the total magnetic field which passes through a given area" [8]. Measuring the voltage across the SQUID can then give an indication of the applied magnetic flux.

A SQUID that is operated without additional control electronics can only measure a very small range of magnetic flux densities with a linear flux-voltage response. A Flux-Locked-Loop (FLL) is therefore required to extend the range of measurable magnetic fields whilst ensuring that the SQUID remains operating in it's linear region.

A FLL operates using negative feedback. The FLL produces a magnetic flux that negates the effect of the applied flux on the SQUID. The output measured from the FLL is a voltage that represents the feedback flux used to negate the applied flux. As such, the output of the FLL is a measure of the change in magnetic flux density rather than a measure of the absolute magnetic flux density seen by the SQUID [1].

1.3 Objectives

The primary objective of this work is to design a Flux-Locked-Loop that can be used to control HTS SQUID sensors for use as magnetometers for low-frequency measurements.

The proposed FLL design should:

1. Accurately track magnetic fields with ultra-low frequencies (in the mHz region).
2. Measure a large range of magnetic flux densities.
3. Be customisable for SQUIDs with different specifications.
4. Allow for both open-loop and closed-loop operation (tuning and measurement).
5. Contribute minimal noise to the SQUID measurements.
6. Implement flux modulation and bias current reversal to improve the noise performance of the SQUID.
7. Be possible to implement using readily available low-cost electronic components.

1.4 Overview

The fundamental concepts behind the operation of SQUIDs as magnetometers are discussed in Chapter 2. An accurate SQUID model is simulated using the JoSIM Superconductor Circuit Simulator to gain a better understanding of a SQUID's response to applied magnetic flux. The results of the simulation are used to model a SQUID with LTspice XVII according to the parameters of the Star Cryoelectronics M2700 magnetometer that the proposed FLL is

designed for. The M2700 is a SQUID magnetometer currently in use at SANSA Space Science in Hermanus, South Africa.

Chapter 3 contains a description of the basic building blocks of a FLL and their individual requirements. The choice of an appropriate power supply is discussed and the design of the proposed system to supply bias current reversal and flux modulation signals is presented. Thereafter the principles behind lock-in detection, integration and feedback are established and the methods of implementing them are described. The remainder of the chapter gives a brief overview of the proposed choice in microcontroller.

The main body of the thesis is in Chapter 4, which focuses on the design of the most important element of the FLL: the low noise pre-amplifier. A number of proposed pre-amplifier designs are explored and evaluated using a combination of hand calculations, LTspice simulations and physical circuit measurements. The chosen pre-amplifier stage for the FLL is then discussed in detail and the design of a subsequent amplification stage with voltage offset removal is investigated.

Chapter 5 contains the results of simulating the full FLL in LTspice. It begins with a discussion of the closed-loop bandwidth of the system and the relationship between bandwidth and noise. Thereafter, the open- and closed-loop response of the proposed FLL is simulated and compared with the expected and desired response for a range of applied flux values. Additional simulations, including the effect of pre-amplifier noise, are performed to determine the suitability of the proposed design for real-world applications.

Chapter 6 concludes the thesis with an evaluation of how well the project requirements were satisfied and a discussion of outstanding challenges, potential improvements and recommendations for future work.

Chapter 2

SQUID Modelling

2.1 The SQUID

At extremely low temperatures, the resistance of certain materials drops to zero and direct current flow through these materials causes no energy loss. This occurs up to a maximum current known as the critical current. For values larger than the critical current, the materials have non-zero resistance and operate normally. This phenomenon of zero resistance at low temperatures is referred to as superconductivity [9].

In addition to the the lack of resistance, all magnetic flux is expelled from the material when it is in its superconducting state. When a loop of superconducting material is placed in a magnetic field and put into its superconducting state, the magnetic flux becomes trapped inside the loop. Removing the applied magnetic field then induces a current in the loop that keeps the flux constant [6].

According to [6], a Josephson junction consists of two layers of superconducting material separated by an extremely thin barrier known as a "weak link". This barrier could consist of a non-superconducting or insulating layer. Alternatively, it could be formed by narrowing the superconductor in this region or by using step-edge grain-boundaries. Below the critical current, electrons from the superconducting layers can "tunnel" through the barrier without resistance. When the critical current of the barrier is exceeded, an AC voltage develops across the Josephson junction.

A DC Superconducting Quantum Interference Device (SQUID) consists of two Josephson Junctions in a superconducting loop. The junctions are shunted by a resistor to prevent hysteresis in the I-V behaviour of the SQUID [1]. The SQUID is biased with a current that is slightly larger than twice the value of the critical current of the Josephson junctions. If external magnetic flux is inductively coupled into the SQUID in this state, changes in the flux will produce changes in the current flowing in the superconducting loop. The current contributes to a change in the voltage across the junctions. This voltage is found to be periodic with applied flux where the period is equal to one magnetic flux quantum $\Phi_0 = 2.0678$ Wb [6].

This relationship between output voltage and applied magnetic flux is what makes the SQUID useful as an extremely sensitive magnetometer. Since the output voltage corresponds to changes in magnetic flux, a SQUID can only be used to measure changes in the magnetic flux density and can't be used to make absolute flux measurements. Throughout the rest of this thesis, magnetic field is used to refer to magnetic flux density in Tesla (T).

There are two types of DC SQUIDS: Low Temperature Superconductor (LTS) and High Temperature Superconductor (HTS). LTS SQUIDs are made out of materials that are superconducting at the boiling point of liquid helium (4.2 K) whereas HTS SQUIDS materials are superconducting at the boiling point of liquid nitrogen (77 K). LTS SQUIDs are more sensitive and have better stability with lower noise than their HTS counterparts [6]. Since liquid helium is expensive and difficult to access, HTS SQUIDs are often preferred for their accessibility.

Figure 2.1 below shows the voltage-flux relationship in an ideal DC SQUID. Since the Josephson junctions are resistively-shunted, the bias current produces a voltage offset in the SQUID's output signal.

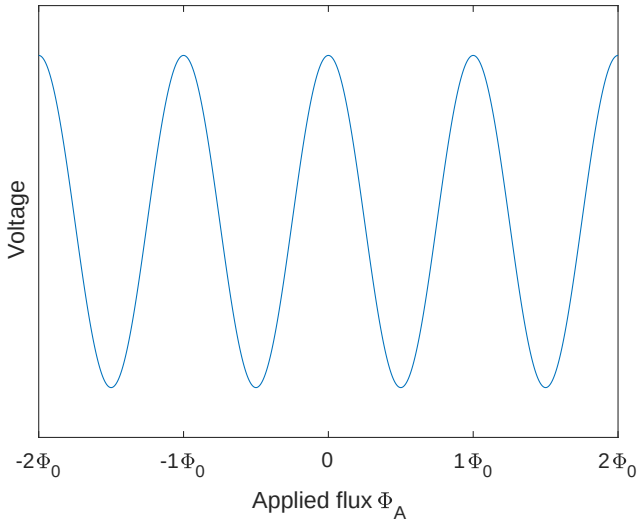


Figure 2.1: Ideal voltage-flux relationship of a DC SQUID.

2.2 JoSIM Model

A complete simulation model for an actual SQUID was obtained from [10]. This model was simulated using JoSIM Superconductor Circuit Simulator to gain a better understanding of a SQUID's response to applied flux at different bias currents. The simulation results obtained from JoSIM show three important plots:

1. I(LCOIL) - Current through the input coil which corresponds to an applied magnetic flux.
2. V(OUT) - The output voltage of the SQUID.
3. V(FILTOUT) - The output voltage of the SQUID after a 3 GHz low pass filter.

Figure 2.2 shows the simulation results when the critical current of each Josephson junction was set to 10 μA. The bias current of the SQUID was stepped from 20 μA to 23 μA with 1 μA steps every 5 ns. Figure 2.3 shows the simulation results when the critical current of each Josephson junction was set to 50 μA. The bias current of the SQUID was stepped from 100 μA to 115 μA with 5 μA steps every 5 ns. From these plots, it is clear that the peak-to-peak output voltage of the SQUID decreases with increasing bias current. The output modulates the most when the bias current is exactly equal to the sum of the critical currents in each Josephson junction.

For correct operation, a SQUID should not be biased at this current. A value that is slightly larger than this should be chosen instead. For the SQUID with Josephson junction critical

currents of 10 μA, 21 μA is a suitable bias current. For the SQUID with Josephson junction critical currents of 50 μA, 102 μA is a suitable bias current.

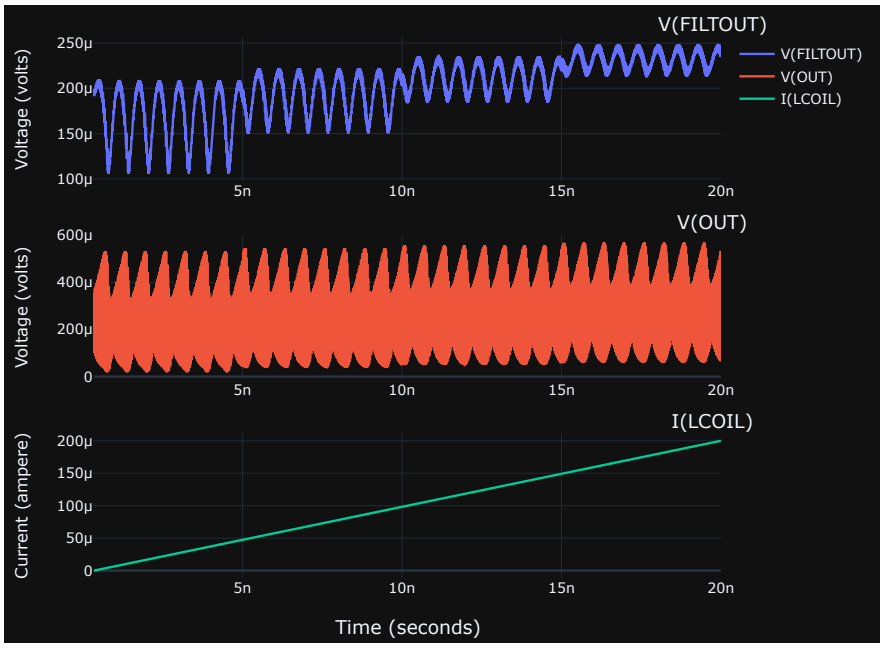


Figure 2.2: JoSIM output of a simulated SQUID with Josephson junction critical current $I_c = 10$ μA for a range of bias currents.

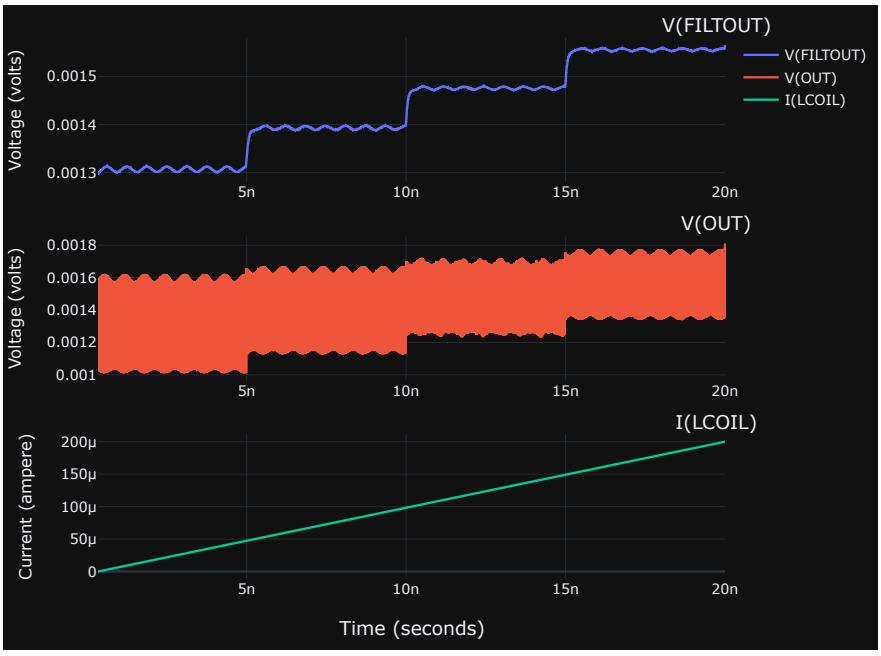


Figure 2.3: JoSIM output of a simulated SQUID with Josephson junction critical current $I_c = 50$ μA for a range of bias currents.

Figure 2.4 shows the results of the simulated SQUID with critical currents of $I_c = 10$ μA that is biased with 21 μA. For this bias current, the SQUID produced a peak-to-peak output voltage of 60.184 μV/Φ_0, a voltage offset of 187.549 μV and a period that corresponded with 6.082 μA/Φ_0 through the input coil. Figure 2.5 shows the results of the simulated SQUID with

critical currents of $I_c = 50$ μA that is biased with 102 μA. With these parameters the SQUID produced a peak-to-peak voltage of 9.903 $\mu V/\Phi_0$, a voltage offset of 1.342 mV and a period that corresponded with 6.066 $\mu A/\Phi_0$ through the input coil.

As expected, the voltage offset increased with increasing bias current through the SQUID resistance. There was also a marked decrease in the peak-to-peak output voltage between the critical current of $I_c = 10$ μA and $I_c = 50$ μA.

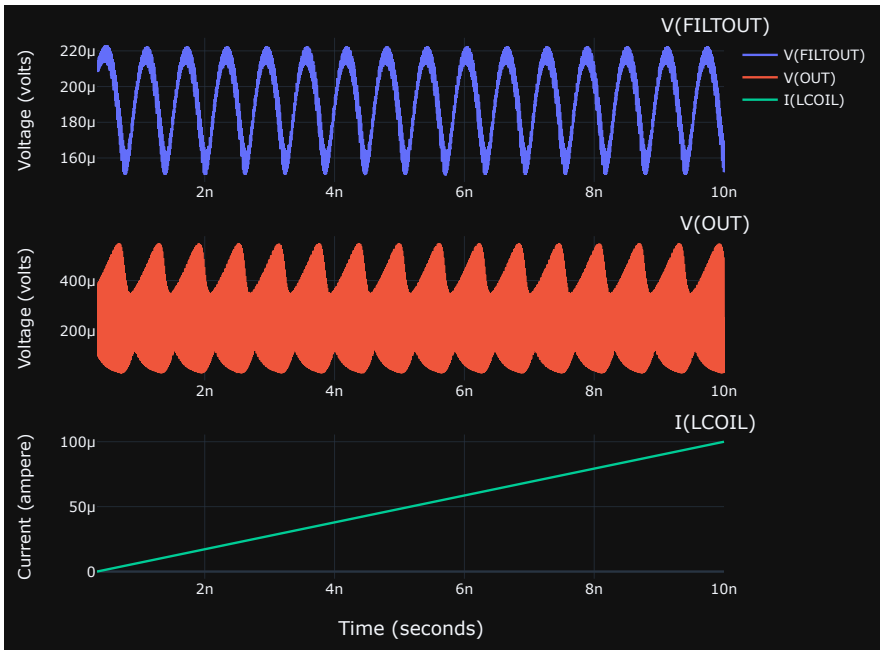


Figure 2.4: JoSIM output of a simulated SQUID with a Josephson junction critical current $I_c = 10$ μA for a bias current of 21 μA.

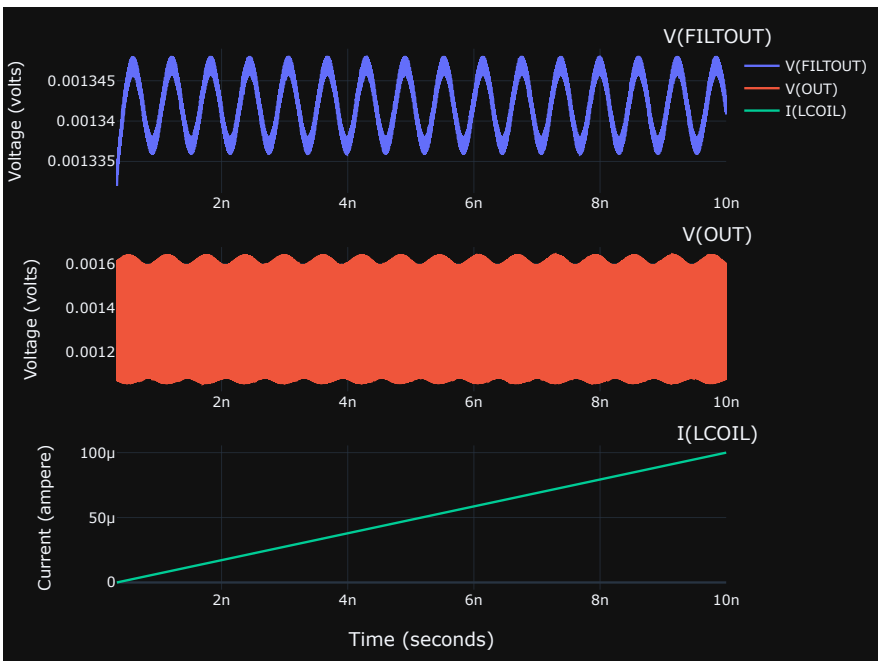


Figure 2.5: JoSIM output of a simulated SQUID with a Josephson junction critical current $I_c = 50$ μA for a bias current of 102 μA.

2.3 M2700 SQUID

The Flux-Locked-Loop in this thesis was designed based on the specifications of the M2700 High-T_c DC SQUID Magnetometer from Star Cryoelectronics [11]. This is the magnetometer that is currently installed at SANSA Space Science in Hermanus, South Africa. It consists of two SQUIDs with a large-area pickup loop connected to the SQUID inductances to increase the sensitivity [6]. The SQUIDs can be operated individually or serially. Only the individual operation was considered for this research.

Table 2.1 contains the useful parameters of the M2700 HTS Magnetometer obtained from [11].

Table 2.1: Specifications of the M2700 SQUID [11].

Parameter	Value		
	Minimum	**Typical**	**Maximum**
SQUID critical current $2I_C$	10 μA	50 μA	100 μA
SQUID resistance $R/2$	-	3 Ω	-
Feedback mutual inductance $1/M_f$	-	17 μA/Φ_0	-
Voltage Swing ΔV	-	30 μV	-
Field Calibration	-	33 nT/Φ_0	-
Field noise $\sqrt{S_B(f)}$, $f > 10$ Hz	-	-	300 fT/$\sqrt{Hz}$

Table 2.2 contains the resistance values obtained from [11] corresponding to the important connection points of the M2700 LEMO package being considered.

Table 2.2: Resistances of the M2700 LEMO package [11].

Connection	Resistance (Ω)
Bias	210
Voltage Output	5
Modulation/Feedback	6

The M2700 sensor package also includes an optional transformer with a 5:1 turns ratio to increase the output voltage of the SQUID without significantly impacting on system noise [3]. When this transformer is used, the resistance at the Voltage Output connection is 125 Ω (5 $\Omega \times 5^2$).

2.4 LTspice Model

LTspice XVII was chosen as the simulation software for the Flux-Locked-Loop due to its large component library and easy-to-use interface. This software does not have functionality for the simulation of superconducting components such as Josephson junctions. As a result, it was necessary to model the SQUID response using arbitrary behavioural voltage sources.

Initially, the response of the JoSIM simulated SQUID was modelled in LTspice to determine if it would function as expected. The current through the input coil was implemented with a simple current source connected to a 1 H inductance (L). The modulating SQUID voltage was modelled as sinusoidal behavioural voltage source with the formula

$$V = -V_{out}\cos(2\pi M_f \times I(L))$$

where V_{out} is half of the peak-to-peak voltage and $1/M_f$ is the current through the input coil that corresponded to one period in the voltage output in Section 2.2. This voltage source was connected to a second source that supplied a constant voltage corresponding to the offset voltage of the SQUID. The output voltage of the SQUID is modelled as being ideal and perfectly sinusoidal for simplification purposes. An actual SQUID response would not exhibit perfectly sinusoidal behaviour.

Figure 2.6 shows the simulation schematic corresponding to the SQUID simulations for each of the two critical currents in Section 2.2. Figure 2.7 shows the results obtained using the simulation schematic in Figure 2.6.

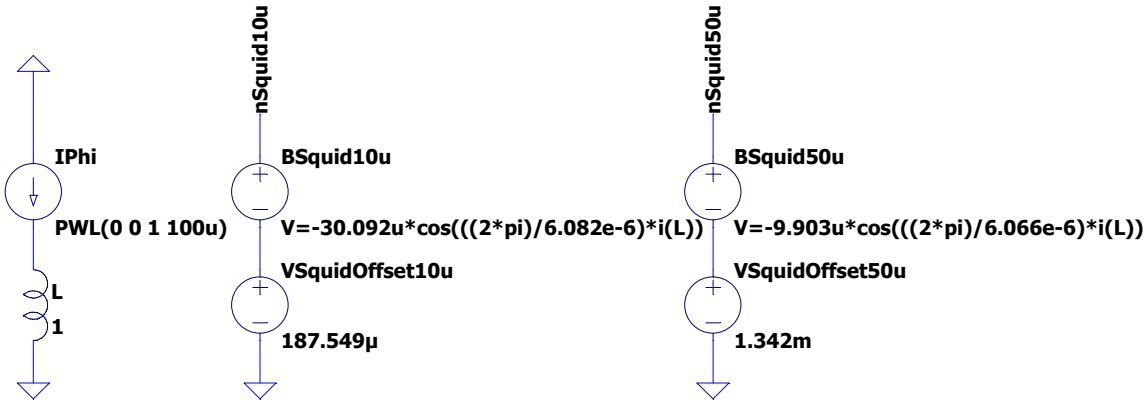


Figure 2.6: LTspice models of the SQUID output voltage from the JoSIM simulations in Section 2.2.

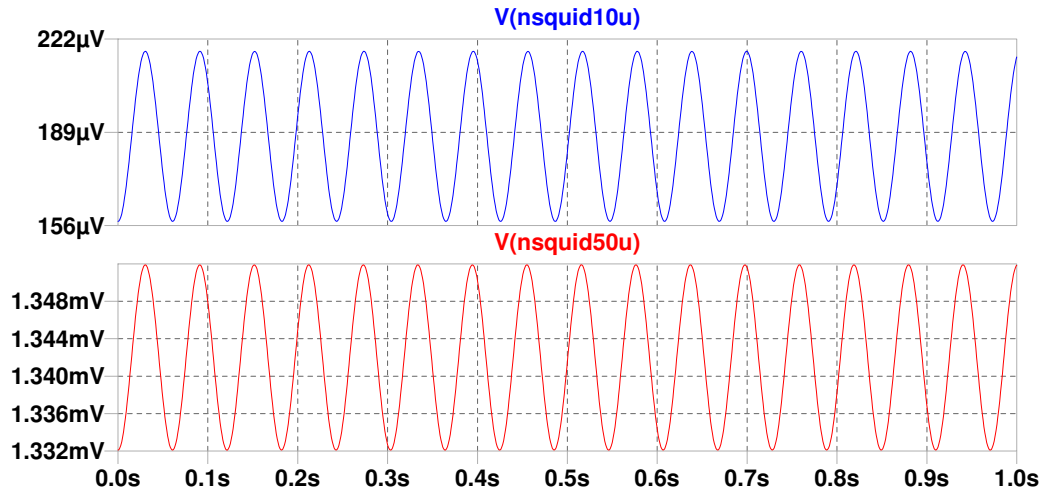


Figure 2.7: LTspice simulation results for the models in Figure 2.6.

The results from the LTspice simulation closely matched the results obtained from the full JoSIM simulation. As such, the same model was used to simulate the behaviour of the M2700 magnetometer according to the parameters mentioned in Section 2.3. The amplitude of the SQUID output voltage was given as 30 μV and the feedback mutual inductance $1/M_f = 17$ μA/Φ_0. The maximum critical current value of 50 μA for each Josephson junction was assumed so that simulations would cater for the largest expected offset voltage. For this critical current value, the bias current of 102 μA that was used in Section 2.2 was chosen. The voltage offset

was then calculated by multiplying this bias current by the resistance measured at the voltage output connections as given in Table 2.2. The assumed voltage offset is thus 510 μV.

Figure 2.8 shows the simulation schematic corresponding to the SQUID simulations for the M2700. Figure 2.9 shows the results obtained using the simulation schematic in Figure 2.8.

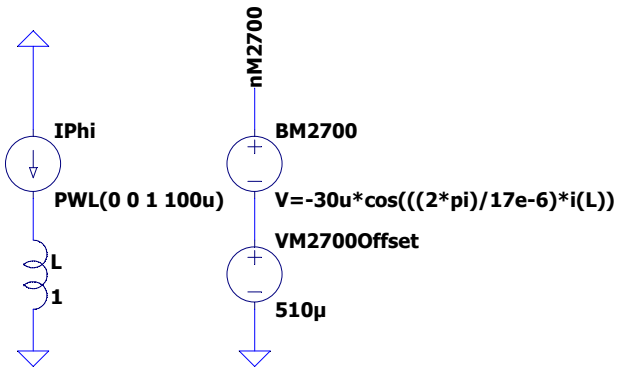


Figure 2.8: LTspice model of the ideal SQUID output voltage for the M2700 using parameters from [11].

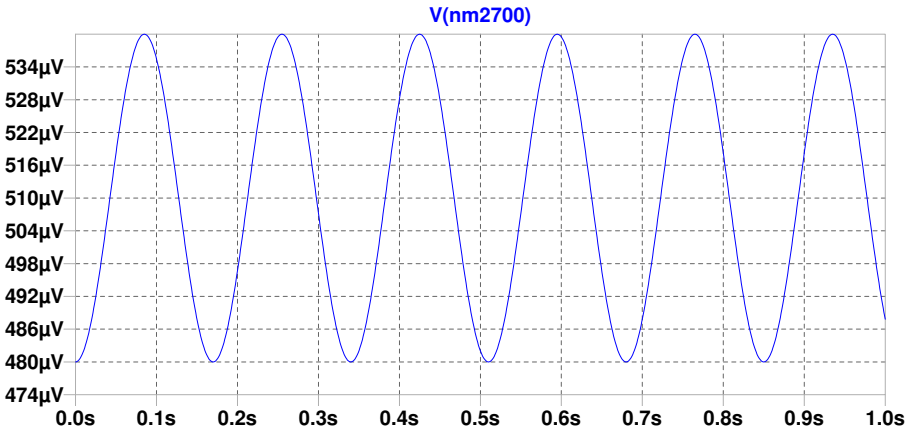


Figure 2.9: LTspice simulation results for the model in Figure 2.8.

Chapter 3

Flux-Locked-Loop

3.1 The Flux-Locked-Loop

The region in which a SQUID has linear V-Φ_A output characteristics is extremely small. This means that the SQUID can only measure small magnetic field ranges (normally less than Φ_0/π) without entering the non-linear region of operation [1]. This limits the output voltage swing of the SQUID. To optimise the voltage swing within the linear region, SQUIDs have to be biased at the steepest part of their V-Φ_A response. This point is known as the working point [1]. In the case of the M2700 magnetometer, the maximum voltage swing is 60 μV_{pk-pk} when the SQUID is biased at its working point [11].

A Flux-Locked-Loop (FLL) is used to increase the range of the SQUID so that it can measure larger magnetic field changes. It operates by amplifying the SQUID's output voltage, integrating it and feeding it back to the SQUID through a feedback resistor and a feedback coil that is magnetically coupled to the SQUID. When the system is in closed-loop operation, the SQUID (which is biased at its working point) is kept at a constant applied flux due to the negative feedback [1]. The voltage across the feedback resistor is then linearly dependent on the applied flux according to R_F/M_f where M_F is the mutual inductance that magnetically couples the feedback coil to the SQUID. In the case of the M2700, $1/M_f = 17\ \mu A/\Phi_0$ [11]. The measurable output voltage in response to magnetic flux is thus dependent on the feedback resistor and mutual inductance, as opposed to the linear range of the SQUID.

Since SQUIDs are such sensitive magnetometers, the impact of noise on the system has to be carefully considered when designing a FLL.

There are two methods of biasing a SQUID: current bias and voltage bias. For current bias, a DC current is passed through the SQUID with a value larger than the sum of the critical currents of the individual Josephson junctions. The voltage output of the SQUID can then be measured. This was the method used in Chapter 2. For voltage bias, the voltage across the SQUID is kept constant and the output current is measured. These two methods have similar noise impacts, but since voltage bias is more complicated to implement and the M2700 is geared towards current bias, current bias was selected for this research.

One of the most commonly-used readout schemes for a FLL is flux modulation. For flux modulation, a square wave flux with a peak to peak value of $\Phi_0/2$ is applied to the SQUID. This flux periodically switches the SQUID between two working points on adjacent slopes of the V-Φ characteristic [1]. Essentially, the output of the SQUID is switched to a higher frequency

where the noise of the sensor is lower. Figure 3.1 shows the two working points of the SQUID for flux modulation.

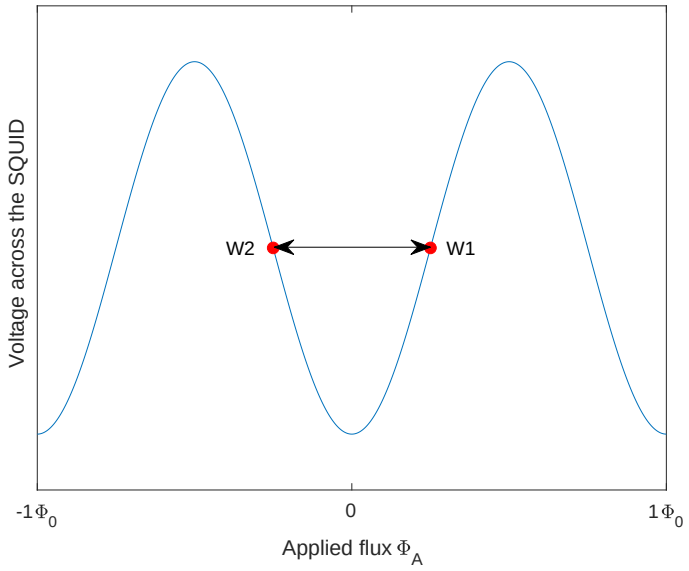


Figure 3.1: Working points of a SQUID for flux modulation.

For HTS SQUIDs like the M2700, fluctuations in the critical current contribute to noise in the SQUID. To minimise this, a technique called bias current reversal is implemented. This technique involves periodically reversing the direction of the SQUID's bias current. This switches the SQUID between working points on its positive and negative voltage-flux characteristics. Figure 3.2 shows the two working points of the SQUID for bias current reversal.

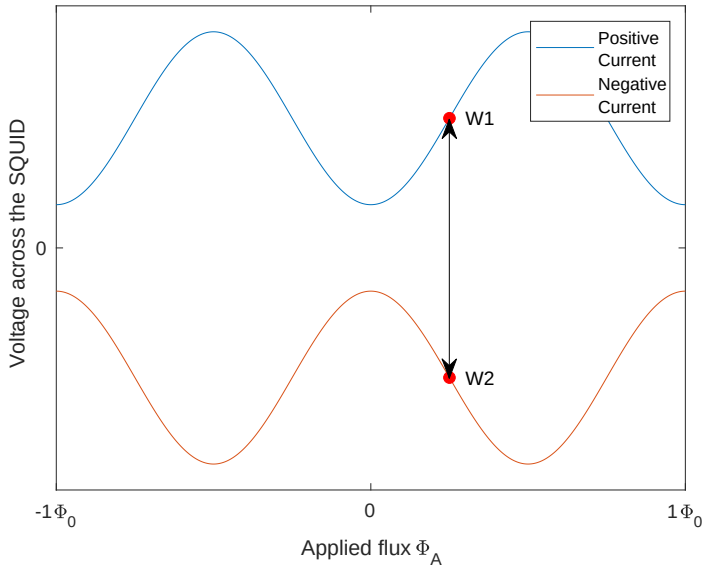


Figure 3.2: Working points of a SQUID for bias current reversal.

When both flux modulation and bias current reversal are implemented, the SQUID is switched between four possible working points as shown in Figure 3.3.

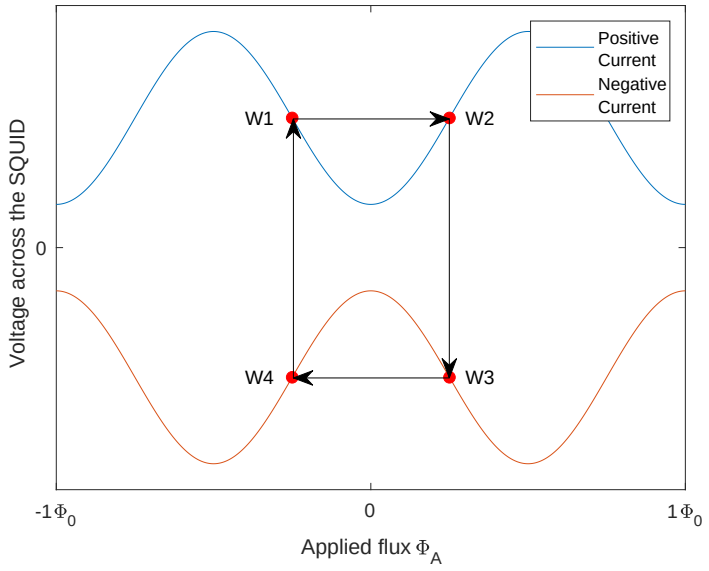


Figure 3.3: Working points of a SQUID with flux modulation and bias current reversal.

When these techniques are used in a FLL, the original signal has to be extracted from the amplified SQUID output before it is integrated and fed back to the SQUID. This is implemented with a lock-in detector that uses the product of the flux modulation and bias current reversal frequencies to detect the original signal in the modulated signal.

Switching the bias current direction also switches the polarity of the offset voltage of the SQUID, making it more complicated to remove the offset from the SQUID measurement. Some systems remove the voltage offset at the point where the SQUID is connected to the FLL using a Digital-to-Analog Converter (DAC) [4]. This is difficult to implement since the noise of the DAC is directly added to the SQUID. An alternative is to remove the offset after the initial low noise pre-amplifier stage where the noise of the DAC would be attenuated by the pre-amplifier's gain.

Figure 3.4 shows a high-level system diagram of the proposed Flux-Locked-Loop design.

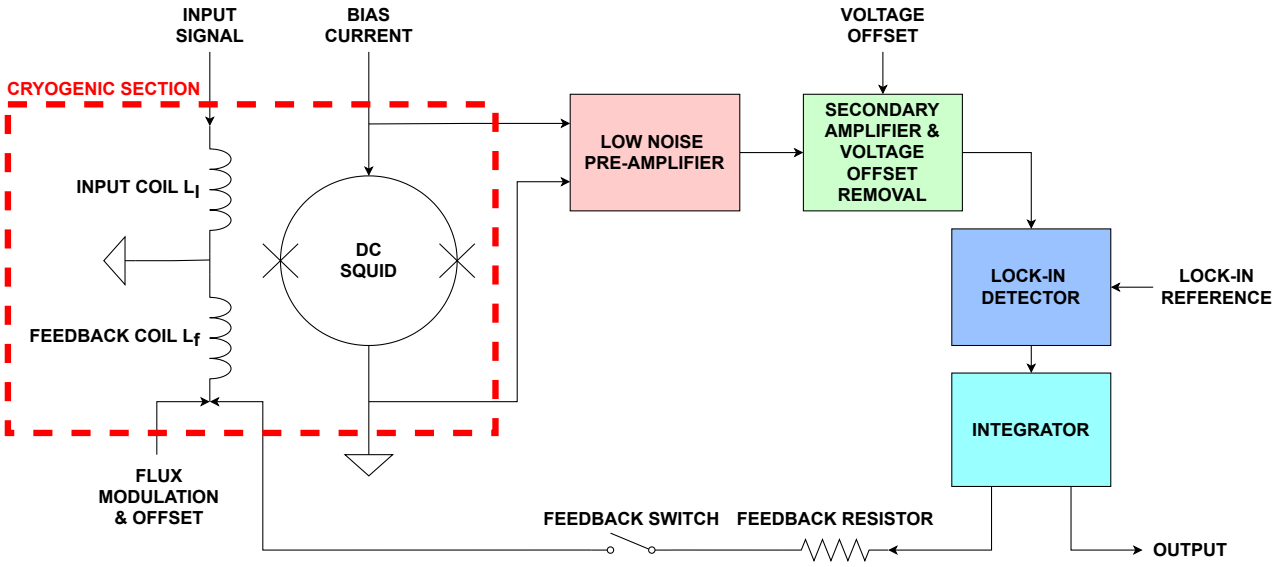


Figure 3.4: High-level system diagram of a Flux-Locked-Loop (FLL).

The design of the low noise pre-amplifier stage and the secondary amplifier with voltage offset removal is discussed in detail in Chapter 4. The remainder of this chapter discusses the choice of power supply for the FLL, the implementation of flux modulation and bias current reversal as well as the design of the lock-in detector, integrator and system feedback. The choice of microcontroller for the FLL is also considered.

3.2 Power Supply

Power supplies are required to provide circuit components with the necessary voltages to operate in the FLL. One important quality of these power supplies is that their noise impact on the circuits is minimal. Both switching and linear power supplies derive their DC output from the 230 V, 50 Hz AC mains supply and are highly susceptible to 50 Hz pickup and noise coupling [12]. In [13], Kim discusses how mixed circuits suffer from noise coupling when noise interference from digital signals affects the analog elements. Since a FLL requires both digital and analog elements, the voltage supplies need to be carefully selected to minimise noise coupling.

According to [14], batteries are suitable power supplies for low noise design. This is because they are isolated and aren't as susceptible to 50 Hz pickup and noise coupling as other power supplies. In [12] the noise of a number of power supplies were tested including a lead-acid battery. The battery had the lowest noise by far of the different power supplies.

Integrated Circuits (ICs) such as the D-type flip-flops and Digital-to-Analog Converters (DACS) that are discussed later in Sections 3.3.2 and 3.3.3 respectively, typically require supply voltages of ± 5 V. The SPST switches, SPDT switch and operational amplifiers used in the lock-in detection, integration and amplification stages (Sections 3.4, 3.5 and Chapter 4) require larger supply voltages, dependent on the desired output voltage range of the FLL. The user manual for the SQUID system from Star Cryoelectronics indicates an integrator output range of ± 10 V [3]. To achieve a similar range, a value of ± 12 V is chosen for the supply voltages.

12 V rechargeable lead-acid batteries are readily available from electronic suppliers, covering a wide range of Ah values. These would be a good option to provide the required ± 12 V supplies. The higher the Ah value, the longer the system could be powered without recharging the battery. Batteries with higher Ah values are considerably more expensive, so it would be necessary to find a compromise between price and usability.

The necessary ± 5 V supplies can be derived from the 12 V batteries using voltage regulators. The LT3045 is an ultralow noise, ultrahigh PSRR positive linear regulator from Analog Devices [15]. The LT3094 is essentially the negative complement of the LT3045 [16]. These voltage regulators have very low RMS noise of 800 nV_{RMS} across a 10 Hz to 100 kHz bandwidth. Additionally they have a very high Power Supply Rejection Ratio (PSRR) of over 90 dB at low frequencies. They have adjustable voltage outputs that are controlled by a resistor (R_{SET}) connected between two of the pins on the chip. For both regulators, a resistance of $R_{SET} = 49.9$ kΩ would provide the desired ± 5 V supplies.

At all points where the voltage supplies are connected to circuit components, inserting decoupling capacitors between the power supply line and ground would be necessary. Decoupling capacitors are used to remove voltage spikes and smooth out DC signals thus providing better regulated voltage supplies to components.

Throughout the rest of this document, V_p refers to the +5 V supply, V_n refers to the -5 V supply, V_{p2} refers to the +12 V supply and V_{n2} refers to the -12 V supply.

3.3 Flux Modulation and Bias Current Reversal

According to [1], the frequency for bias current reversal should be considerably larger than the $1/f$ noise corner frequency of the SQUID (see Chapter 4 for a description of noise types). It is also mentioned in [1] that for HTS SQUIDs with flux modulation the typical corner frequency is close to $f_C \approx 1$ kHz.

Since the focus of this work is on low-frequency SQUID measurement systems, $1/f$ noise is a big concern. Choosing a bias current reversal frequency larger than 1 kHz seems desirable since it will limit the effect of the SQUID's $1/f$ noise by switching the output voltage to a higher frequency, but interference from 50 Hz power lines can dominate measurements of low-frequency signals when SQUIDs are not operated in extremely well-shielded environments.

The frequency of the lock-in detection reference is derived from the product of the flux modulation and bias current reversal frequencies. On the advice of Michal Janošek (Assistant Professor at the Czech Technical University in Prague), the frequency of the lock-in detection reference was chosen to be lower than 50 Hz in an attempt to avoid the power line interference [17]. Since the noise of the M2700 SQUID was 300 fT/$\sqrt{Hz}$ for frequencies as low as 10 Hz, the $1/f$ corner frequency is assumed to be sufficiently low for the sub 50 Hz choice.

There are two commonly-used options for selecting the frequency of the flux modulation signal: either as an integer multiple of the bias current reversal frequency or with the same frequency but a phase shift of 90° [1]. It is easier to generate a single frequency and phase shift it by 90° than to generate two frequencies that are well synchronised. As a result, the single frequency with 90° phase shift was chosen.

Since the lock-in detection frequency is obtained by multiplying the bias current reversal and flux modulation frequencies, these frequencies need to be half of the chosen lock-in detection frequency. A frequency of approximately 45 Hz was chosen for lock-in detection and so the flux modulation frequency and bias current reversal frequencies are $f_M = f_B = 22.5$ Hz.

To implement flux modulation, a square-wave current is passed through the feedback coil of the SQUID. The peak-to-peak value of this current should modulate the magnetic flux linking the SQUID by $\Phi_0/2$ [6]. The required current is determined by multiplying the $1/M_f$ value for the SQUID under consideration with $\Phi_0/2$. Since the sinusoidal response of the SQUID is not guaranteed to have a trough at an integer value of the applied flux, an additional current through the feedback coil is required to provide a flux offset as necessary. The value of this current depends on the particular SQUIDs being used.

For the M2700 SQUID, a peak-to-peak current of 8.5 μA is required. As discussed in Section 2.4, the bias current amplitude is chosen as 102 μA.

The remainder of this section discusses the method for generating the reference signal used for lock-in detection as well as the frequencies used for bias current reversal and flux modulation. It also considers the method of generating the required currents.

3.3.1 Reference Signal Generation

Many microcontrollers can generate Pulse Width Modulation (PWM) output signals on their digital output pins. These are signals that switch between full output voltage (digital 1) and zero output voltage (digital 0) at a set frequency. Dividing the duration of time that the signal is at high voltage by the period of the PWM signal gives a percentage value known as the duty

cycle. A duty cycle of 50% indicates that the output is at high voltage for half a period and at zero voltage for the other half. Microcontrollers allow the user to control the frequency and duty cycle of the PWM output signal. This means that a microcontroller could be used to supply the square wave reference signal used for modulation and lock-in detection. This functionality was tested using an Arduino Leonardo development board.

The Arduino Leonardo is a development board that uses the ATmega32U4 microcontroller produced by Atmel. It has a 16 MHz crystal oscillator providing the base clock signal and 7 of its 20 digital output pins can support PWM. The output pins can supply up to 40 mA of current [18]. The ATmega32U4 has four timers which are used to control PWM outputs: one 8-bit timer (Timer0), two 16-bit timers (Timer1 and Timer3) and one 10-bit high-speed timer (Timer4). These timers all have separate prescalers and multiple output compare units controlled by the timer registers [19].

The 8-bit and 16-bit timers have a prescaler options of 1, 8, 64, 256 or 1024 while the 10-bit high-speed timer only has options of 1, 2, 4 or 8. The frequency at which the timers count is determined by dividing the base clock signal of the microcontroller by the chosen prescaler. For the 8-bit and 16-bit timers, the lowest operating frequency is 15.625 kHz using 1024 as the prescaler. For the 10-bit high-speed timer, the lowest operating frequency is 2 MHz using 8 as the prescaler. The 8-bit and 16-bit timers are therefore far more suitable for producing the desired sub 50 Hz PWM output.

The Arduino Leonardo has its 8-bit Timer0 mapped to digital pins 3 and 11. Pin 3 can also function as the Serial Interface Clock in a 2-wire serial interface, and should be left available in case this functionality is required. In addition, Timer0 is often used to control the delay() function of an Arduino so changing its register values can lead to unexpected behaviour. Therefore, the 16-bit timers are more suitable than the 8-bit timer for generating the PWM signal.

The number of bits used for the timer determines what maximum value the timer can count up to before resetting/counting down. For a 16-bit timer this maximum value is 65535. By default, the top value that the timer counts up to is set to the maximum. This top value also determines the lowest frequency of the PWM output, and so changing it allows for an adjustment of the frequency of this output.

To generate a PWM signal, the count of the timer is constantly compared to a value stored in an Output Compare Register (OCRn). If the timer count matches this value, the voltage on the pin corresponding to that register is set high or low according to a setting in the timer registers [20].

The 16-bit timers have three modes of operation for PWM output: Fast PWM, Phase-correct PWM and Phase and Frequency correct PWM. For Fast PWM, the timer counts from 0 to the top value and then restarts at 0. For Phase-correct PWM, the timer counts from 0 to the top value and then back down to 0. This allows for more symmetrical outputs signals and lower frequencies than Fast PWM.

Phase and Frequency correct PWM operates in a similar way to Phase-correct PWM, but it is preferred when the top value of the timer is changed during operation (frequency changed while the PWM signal is being output). In Phase-correct PWM, the register that stores the top value is updated when the timer reaches the previous top value. As a result, the down count still uses the old top value, but the subsequent up count uses the new top value. This leads to an unsymmetrical output. In Phase and Frequency correct PWM, this register is updated at 0 instead. Since the frequency of the PWM signal does not need to be changed during operation,

the use of Phase and Frequency correct PWM is unnecessary and Phase-correct PWM can be used [19].

The timers have a setting that allows the user to set the top value to the default or to some custom value between 0 and the maximum. Selecting the second option enables the user to perform additional frequency manipulation beyond that obtained by just using the prescaler. When this option is chosen, the top value is set to the value stored in Output Compare Register A for the chosen timer. Since this same value is used to produce the PWM signal for the corresponding Output Compare pin, this means that this pin will always have a duty cycle of 50% and a frequency determined by the value in the register. If a different duty cycle is needed, the output of another output compare pin corresponding to this timer can be used since its Output Compare Register can be changed without affecting the timer. In this case a duty cycle of 50% is desired and only one frequency is needed, so only one pin is required to produce the output. Figure 3.5 shows how the desired PWM signal is produced using a top value of 85 from Output Compare Register A.

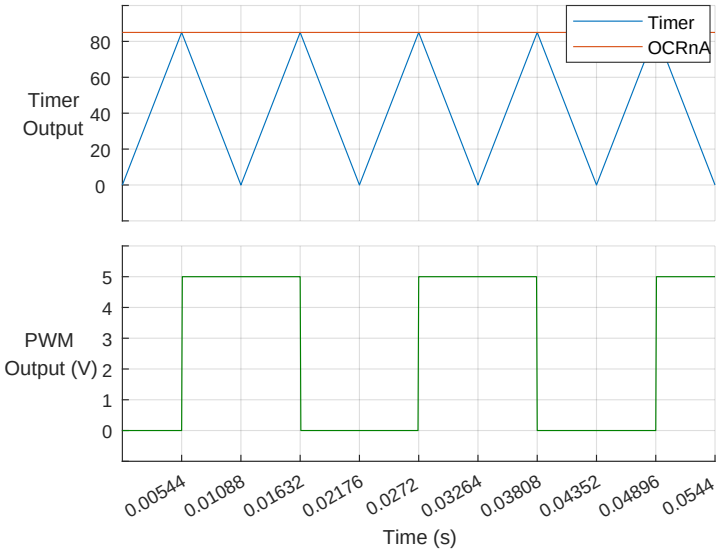


Figure 3.5: Representation of the method used by an Arduino to generate a Phase-correct PWM signal. The output pin is toggled when the timer matches the value stored in OCRnA (85).

Timer1 of the ATmega32U4 has all three of its output compare pins mapped to digital pins on the Arduino (pins 9, 10 and 11). Timer3 only has one output compare pin mapped to an Arduino pin (pin 5). Since only one pin is required and pin 5 is not mapped to anything else, Timer3 is the best option. The PWM output can then be manipulated by setting bits in the Timer/Counter3 Control Registers (TCCR3A and TCCR3B).

The first step is to set the timer mode to Phase-correct PWM where the top value is equal to the value stored in the Output Compare Register for channel A (OCR3A). According to Table 14-4 in the datasheet, the Waveform Generation Mode (WGM3) bits need to be set to 1011 to achieve this. Next the Compare Output Mode bits for Channel A (COM3A) need to be set to toggle the Output Compare pin for Channel A (OC3A/pin 5) when the counter matches the value in OCR3A. From Table 14-3 in the datasheet, the COM1A bits need to be set to 01 to achieve this. Then the Clock Select bits (CS3) need to be set to 101 to provide the initial 1024 clock prescaler. Thereafter, the value of the Output Compare Register (OCR3A) can be set to

provide the desired frequency for the PWM output. Setting OCR3A to 85 produces a PWM output frequency of 45.956 Hz which is close to the chosen output frequency of 45 Hz. This value is calculated from:

$$f = \frac{16 \times 10^6}{1024 \times 2 \times 2 \times OCR3A}. \tag{3.1}$$

The COM3A bits and the last two bits of WGM3 are stored in register TCCR3A while the first two bits of WGM3 and the CS3 bits are stored in register TCCR3B. The default state of all bits in the two registers is 0. The following code is used to set the bits in the registers to the desired values. This code is placed in the setup() block of the Arduino so that it produces a continuous output and is not affected by delays in the main while loop. The code extract below shows how to set up the signal.

```
TCCR3A = _BV(COM3A0) | _BV(WGM31) | _BV(WGM30);
TCCR3B = _BV(WGM33) | _BV(CS32) | _BV(CS30);
OCR3A = 85;
```

Figure 3.6 shows the Arduino PWM signal measured with an oscilloscope on the output pin. The Arduino produced a square wave that switched between 0 V and 5.16 V as desired. A multimeter was used to measure the frequency and duty cycle of the PWM signal. The frequency was measured as 45.95 Hz and the duty cycle as 50%. This closely matches the desired output and indicates that the Arduino may be a good way of producing the required reference signal.

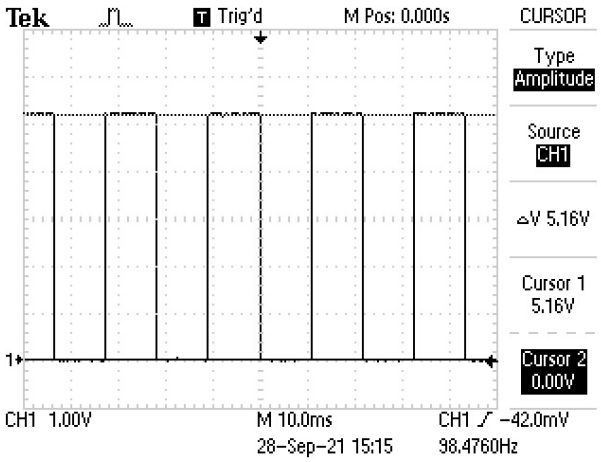


Figure 3.6: Oscilloscope measurement of the Arduino Leonardo's PWM output.

Figures 3.7 and 3.8 show the point at which the voltage output switches from low to high as measured with an oscilloscope. In Figure 3.7 the cursors were used to measure the settling time, $t_s = 188$ ns. In Figure 3.8 they were used to measure the overshoot, $V_{over} = 2.64$ V. The settling time is very low which is desirable, but the overshoot is quite high at over 52% of the settled output voltage. Since measurements were taken without using appropriate probes with the capacitance tuned out, the excessive overshoot was likely caused by the measurement equipment. If the overshoot is still excessive using appropriate probes, a RC low-pass filter can be included at the Arduino's output to reduce it. The RC filter has an added consequence of increasing the settling time, but since t_s is low, this would be a reasonable design choice. The measured results indicate that an Arduino could provide the required reference signal.

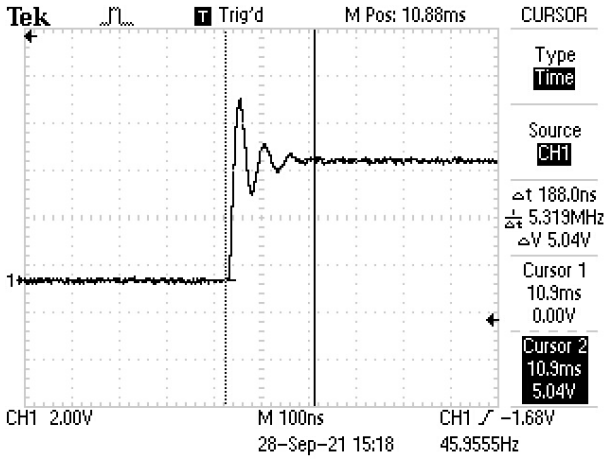


Figure 3.7: Oscilloscope measurement of the settling time of the Arduino Leonardo's PWM output.

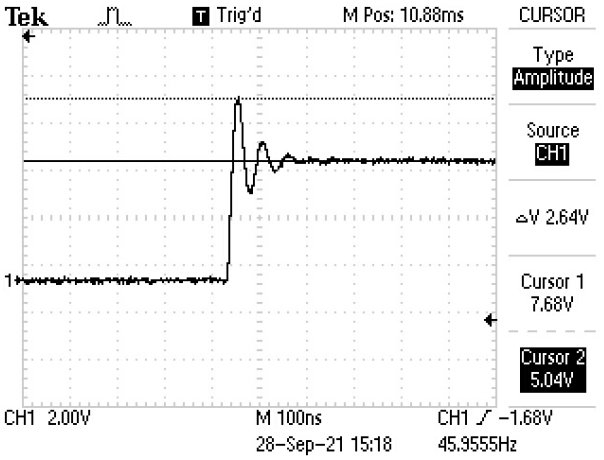


Figure 3.8: Oscilloscope measurement of the overshoot of the Arduino Leonardo's PWM output.

3.3.2 Digital Phase Splitter

A Digital Phase Splitter is used to produce two output signals with the same frequency and a 90° phase shift between them. The frequency of these output signals is half that of the input signal. This makes a Digital Phase Splitter ideal for generating the flux modulation and bias current reversal frequencies from the reference signal frequency which can be used for lock-in detection. This method of phase shifting is only used for digital input signals. Since the PWM output of the Arduino is a square wave that switches between digital 0 (0 V) and digital 1 (5 V), it can be considered a digital signal and can be phase shifted using this method.

A Digital Phase Splitter is normally constructed using two identical positive-edge-triggered D-type flip-flops and an inverter as in [21]. The input signal is connected to the clock input of one of the flip-flops and the inverter. The output of the inverter is connected to the clock input of the second flip-flop. For each of the flip-flops, the Data (D) and inverted output ($\overline{Q}$) are connected together and the output is available at the normal output (Q). Table 3.1 shows the operation of each flip-flop in the Digital Phase Splitter. From this table, it is evident that the flip-flop with the inverter has the same response as a negative-edge-triggered flip-flop without an inverter when connected in the same configuration.

Table 3.1: Operation of D-type flip-flops in a Digital Phase Splitter.

Flip-flop without inverter				**Flip-flop with inverter**			
Inputs		**Outputs**		**Inputs**		**Outputs**	
CLK	**D**	**Q**	$\overline{\mathbf{Q}}$	**CLK**	**D**	**Q**	$\overline{\mathbf{Q}}$
H	X	Q	$\overline{Q}$	H	X	Q	$\overline{Q}$
L	X	Q	$\overline{Q}$	L	X	Q	$\overline{Q}$
↑	L	L	H	↑	X	Q	$\overline{Q}$
↑	H	H	L	↑	X	Q	$\overline{Q}$
↓	X	Q	$\overline{Q}$	↓	L	L	H
↓	X	Q	$\overline{Q}$	↓	H	H	L

Figure 3.9 shows the design of a Digital Phase Splitter with one positive-edge-triggered flip-flop

and one negative-edge-triggered flip-flop.

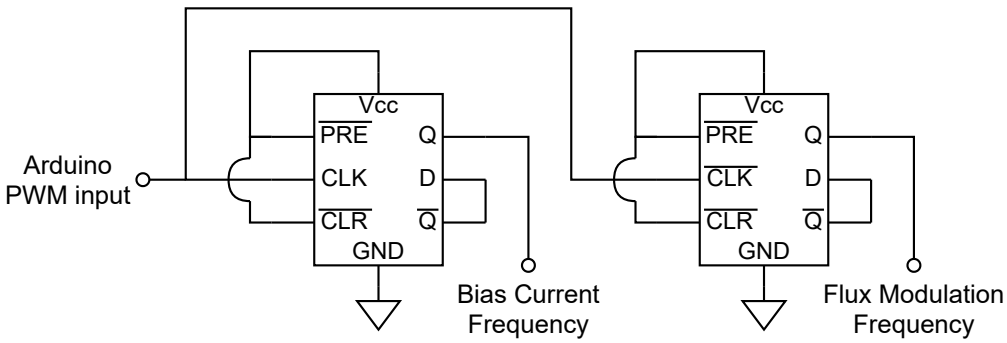


Figure 3.9: Circuit Diagram of a Digital Phase Splitter using two D-type flip-flops.

The SN74HCS74 Positive-Edge-Triggered D-type flip-flop and its counterpart, the SN74HCS72 Negative-Edge-Triggered D-type flip-flop from Texas instruments would be suitable for this application [22] [23]. They have very fast switching times (less than 100 ns), operate using $V_{CC} = 5$ V which can be obtained from the voltage regulator in Section 3.2 and are readily available from electronics suppliers. These flip-flops include Clear and Preset functionality which is not required in this case. Since the pins are active low, they can be tied to V_{CC} so that they remain permanently inactive.

Figure 3.10 shows the expected output of the design in Figure 3.9 for an input PWM signal from an Arduino as calculated in Section 3.3.1. This circuit design would be suitable for producing the required flux modulation and bias current reversal frequencies.

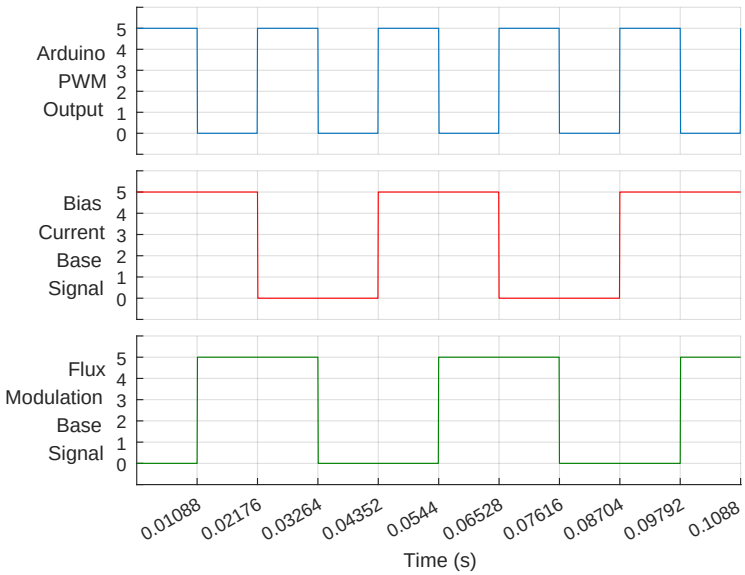


Figure 3.10: Expected output of the design in Figure 3.9 for an input PWM signal from an Arduino as calculated in Section 3.3.1.

3.3.3 Current Source DACs

In order to convert the square-wave voltage output obtained from the Digital Phase Splitter to a controllable current, a multiplying current output Digital-to-Analog Converter (DAC) is

required. A range of DACs that were readily available from electronics suppliers were considered. The list was narrowed down to those with the highest resolutions and current ranges that could accommodate the small output currents required (under 150 μA). The DAC8812 produced by Texas Instruments was chosen as the most suitable option.

The DAC8812 is a dual 16-bit multiplying current output DAC with a low voltage noise of 12 nV/$\sqrt{\text{Hz}}$ in the flatband and a full-scale output current of 2 mA for a reference signal of 10 V [24]. For this reference, the minimum output current increment is

$$\frac{2\times10^{-3}}{2^{16}} = 30.5 \text{ nA}$$

The DAC8812 is a four quadrant multiplying DAC which means that it can produce an AC output from an AC reference signal [25]. However, since the DAC8812 is powered by a single supply voltage of +5 V, it cannot produce bidirectional current output unless a dual supply operational amplifier is connected at its output. The operational amplifier acts as a current to voltage converter, which results in the current output DAC acting as a voltage output DAC. Since a programmable current is required, this is not the desired result. In the datasheet for the AD5545/AD5555 dual 16-bit multiplying current output DACS from Analog Devices, a method of using the DACS for a programmable bidirectional current source is detailed [26].

This method involves converting the voltage output of the operational amplifier at the DAC's output back into a current using an improved Howland Current Pump circuit. As discussed in [26], the programmable current source could supply current to a load of up to 500 Ω. The resistance across the biasing pins of the SQUID is given as 210 Ω and the resistance across the modulation pin is given as 6 Ω [11]. These values are both well under the 500 Ω maximum load mentioned in the datasheet which indicates that this circuit configuration might be suitable.

Figure 3.11 shows the circuit diagram of the programmable current source with an improved Howland Current Pump. The load resistance was chosen as 220 Ω (a standard resistor value close to the 210 Ω at the SQUID biasing pins). With D as the digital value sent to the DAC, the output current of the circuit is calculated as [26]:

$$I_{LOAD} = \frac{\frac{R_2+R_3}{R_1}}{R_3} \times V_{REF} \times \frac{D}{2^{16}} \tag{3.2}$$

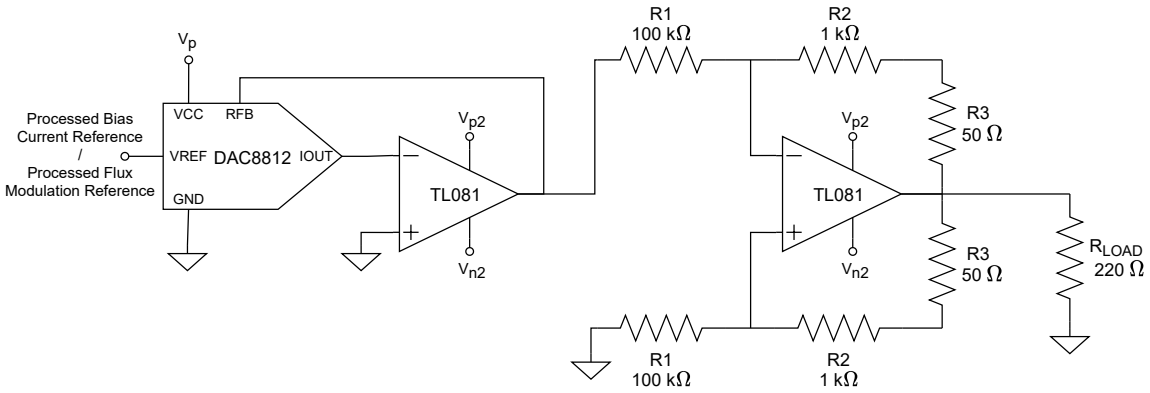


Figure 3.11: Circuit configuration of a programmable current source using the DAC8812 and an improved Howland Current Pump as recommended in [26].

Resistor values were chosen to produce a full-scale output current close to the full-scale output of the DAC8812 for a 10 V reference: $R_1 = 100$ kΩ, $R_2 = 1$ kΩ and $R_3 = 50$ Ω. These values

produce a full-scale output of 2.1 mA through the load for a reference signal of 10 V. The minimum output current increment is thus

$$\frac{2.1\times10^{-}3}{2^{16}} = 32.0 \text{ nA}$$

The DAC8812 is controlled using a three wire serial interface with Chip Select ($\overline{\text{CS}}$), clock (CLK) and a data line (SDI). As in Section 3.3.1, the available Arduino Leonardo was used to test the functionality of the programmable current source. The Arduino Leonardo has Serial Peripheral Interface (SPI) communications supported on its In-Circuit Serial Programming (ICSP) header [18]. This includes a pin for Master Out Slave In (MOSI), Master In Slave Out (MISO) and serial clock (SCK) [27]. Since no information is passed from the DAC8812 to the Arduino, the MISO pin is not required. The MOSI pin is connected to the SDI pin of the DAC8112, and the SCK pin is connected to the CLK pin of the DAC8112. The Arduino has no specific pin corresponding to $\overline{\text{CS}}$ of the DAC8812, but any digital output pin can be used. This $\overline{\text{CS}}$ pin is pulled low to initiate SPI communications.

The DAC8812 has three additional control pins: the $\overline{\text{LDAC}}$ pin, the $\overline{\text{RS}}$ pin and the MSB pin. The $\overline{\text{LDAC}}$ pin is pulled low to transfer data from the input registers to the DAC registers after SPI communication has taken place. This simultaneously updates both DACs on the chip. The $\overline{\text{RS}}$ pin is pulled low to reset the input and DAC registers to zero-scale or mid-scale depending on the state of the MSB pin. If the MSB pin is set high, it resets to mid-scale. If it is set low then it resets to zero-scale. The $\overline{\text{LDAC}}$ and $\overline{\text{RS}}$ pins are connected to digital output pins on the Arduino. In this case the MSB pin is tied to GND so that the system always resets to zero-scale when $\overline{\text{RS}}$ is pulled low.

The Arduino Leonardo can communicate with a clock frequency of up to 16 MHz. Since the maximum clock frequency at which the DAC8812 can operate is 50 MHz, SPI communication between the two is possible. The Arduino SPI library is used to control communications [27].

For the DAC8812, data is clocked in MSB first with only the last 18 bits considered. Since the Arduino sends SPI communications one byte at a time, three bytes are required to store the 18 bits. The last two bits of the first byte control which of the two DACs is selected. The other 6 bits are ignored by the DAC. The second byte contain the first 8 bits of the 16-bit data value that controls the DAC output. The last byte contains the last 8 bits of the 16-bit data value [24].

The Arduino has to be set up to send data according to the format understood by the DAC8812. This is done using the SPI.beginTransaction(SPISettings (P1, P2, P3)) command. The first parameter (P1) is the frequency used for communication, the second parameter (P2) specifies if the data is sent MSB first or LSB first. The last parameter (P3) selects the mode for data communication (whether the data is shifted on the rising or falling edge and whether the clock is idle low or high). P1 is chosen as 16 MHz (the Arduino maximum) and P2 is set to MSBFIRST. The table in [27] and the DAC8812 datasheet [24] are used to determine the appropriate mode. The data is shifted in on a rising clock edge and the clock is idle high so SPI_MODE3 is chosen.

The process to set the value of one of the DACs on the DAC8812 is as follows:

1. The $\overline{\text{CS}}$ pin is pulled low.
2. The first byte containing the bits to select the DAC is transferred.
3. The second byte containing the first 8 bits of the data value is transferred.
4. The third byte containing the last 8 bits of the data value is transferred.

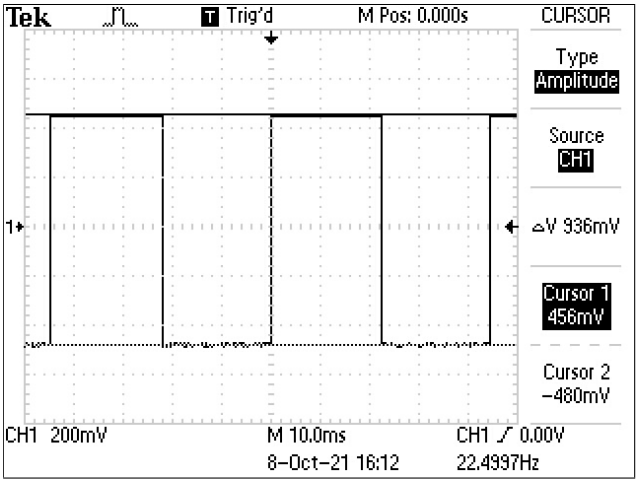
5. The $\overline{\text{CS}}$ pin is pulled high.
6. The $\overline{\text{LDAC}}$ pin is pulled low.
7. The $\overline{\text{LDAC}}$ pin is pulled high.

The Arduino code required to control the DAC8812 is shown here:

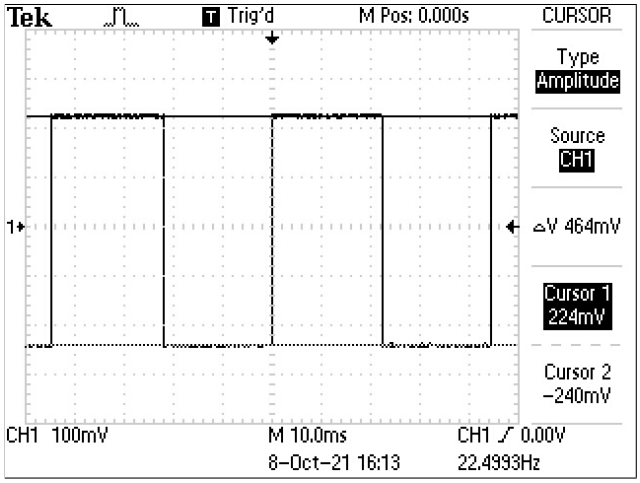
```
#include <SPI.h>

const int CS = 2;
const int LDAC = 3;
const int RS = 4;

void setup() {
  pinMode(CS, OUTPUT);
  pinMode(LDAC, OUTPUT);
  pinMode(RS, OUTPUT);
  digitalWrite(CS, HIGH);
  digitalWrite(LDAC, HIGH);
  digitalWrite(RS, HIGH);
  SPI.begin();
}

void loop() {
  SPI.beginTransaction(SPISettings (16000000, MSBFIRST, SPI_MODE3));
  digitalWrite(CS, LOW);
  SPI.transfer(0x01);
  SPI.transfer(0xFF);
  SPI.transfer(0xFF);
  digitalWrite(CS, HIGH);
  digitalWrite(LDAC, LOW);
  digitalWrite(LDAC, HIGH);
  SPI.endTransaction();
}
```

The circuit in Figure 3.11 was built and tested using readily available components. TL081 operational amplifiers were used for both the current to voltage converter and the improved Howland Current Pump. The +5 V regulated power supply was used for the DAC8812 and the operational amplifiers were powered with the +12 V and -12 V supplies provided by the batteries as discussed in Section 3.2. A signal generator was used to provide the reference voltage to the DAC8812. The signal generator was set to provide a 20 V_{pk-pk} square wave with a frequency of 22.5 Hz (roughly the output frequency of the Digital Phase Splitter). The output of the signal generator was measured and found to switch between 10 V and -10.6 V so a slight imbalance in the output of the circuit was expected.

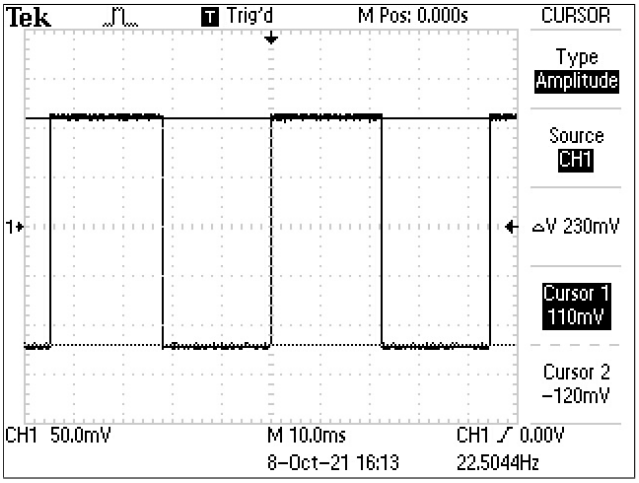
Figure 3.12 shows the voltage outputs measured across the load using an oscilloscope for a range of digital input codes sent from the Arduino. Once again, the measurements were taken without using appropriate probes with the capacitance tuned out.



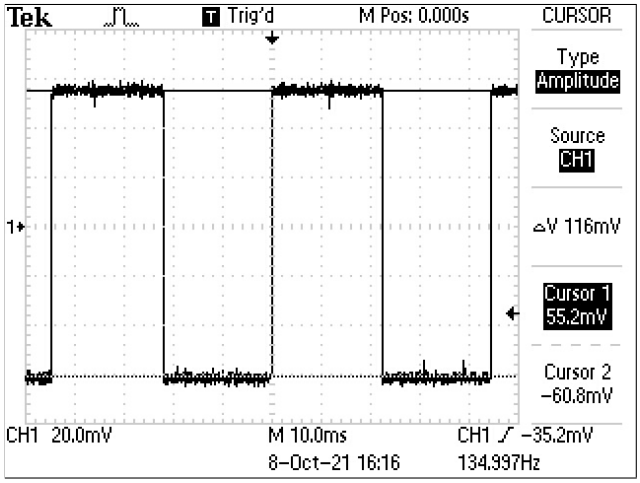
(a) Voltage output for code FFFF



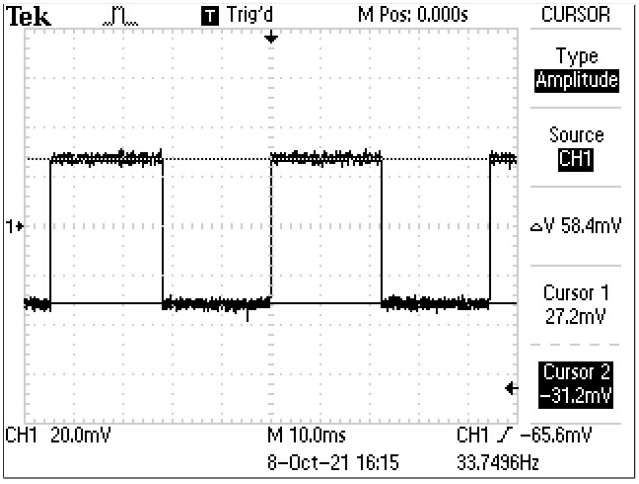
(b) Voltage output for code 8000



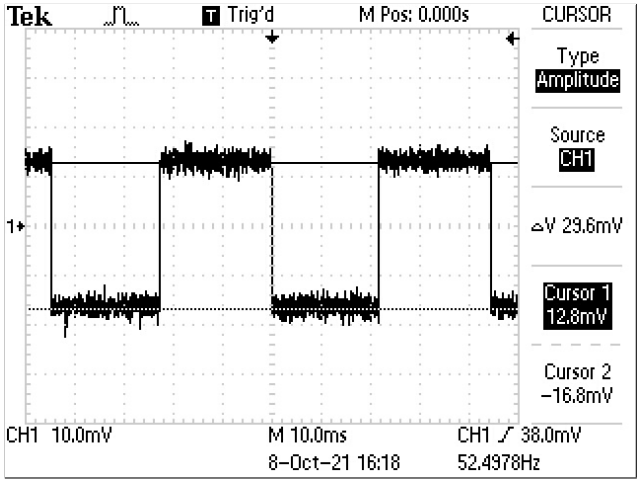
(c) Voltage output for code 4000



(d) Voltage output for code 2000



(e) Voltage output for code 1000



(f) Voltage output for code 0800

Figure 3.12: Voltage output of the DAC8812 current output DAC with improved Howland Current Pump measured across a 220 Ω load resistance using an oscilloscope.

Table 3.2 contains the expected and measured current outputs of the programmable current source corresponding with the plots in Figures 3.12a to 3.12f. The measured results correspond well with the expected results. The differences in expected and measured currents were small considering that high tolerance resistors were used.

Table 3.2: Comparison of measured programmable current source outputs with expected values for a range of digital control codes.

Digital Code Input	10 V Reference		-10.6 V Reference	
	Expected Current	Measured Current	Expected Current	Measured Current
FFFF	2.100 mA	2.073 mA	2.226 mA	2.182 mA
8000	1.050 mA	1.018 mA	1.113 mA	1.091 mA
4000	525 μA	500 μA	565.5 μA	545.455 μA
2000	262.5 μA	250.9 μA	278.25 μA	276.364 μA
1000	131.25 μA	123.64 μA	139.125 μA	141.818 μA
0800	66.625 μA	58.182 μA	69.5625 μA	76.636 μA

Figure 3.13 shows the measured settling time of the programmable current source's output when the reference voltage switches from -10.6 V to 10 V and the DAC is set to full-scale output. The signal takes a little under 4 μs to settle at the new value. This is much larger than expected. The datasheet of the DAC8812 indicated a settling time of 0.5 μs from zero-scale to full-scale output. For switching bidirectionally, a settling time of 1 μs would be expected.

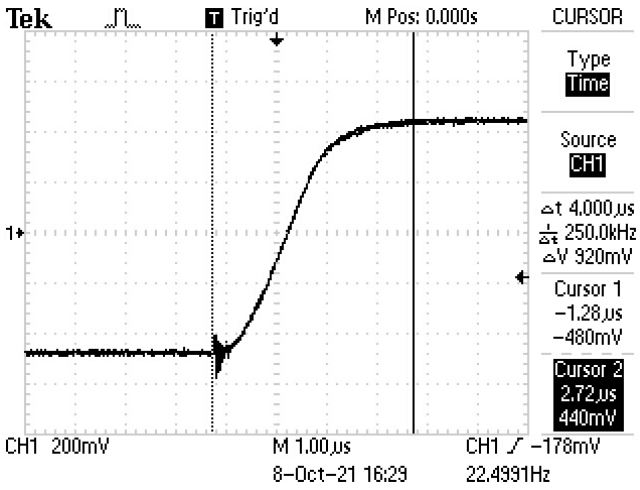


Figure 3.13: Oscilloscope measurement of the settling time of the programmable current source for a reversal of the current at full-scale output.

According to the datasheet, the TL081 opamps normally have high slew rates of 20 V/μs, but in some cases that value can drop as low 5 V/μs [28]. In the case of the operational amplifier used for the current to voltage converter at the DAC's output, the output voltage switches from -10.6 V to 10 V. At a slew rate close to 5 V/μs, this would result in the measured settling time of $t_s \approx 4\mu$s. The oscilloscope probes used would have also contributed to a longer settling time.

The measured output voltage appears to be quite noisy for low current values. In [26], there are guidelines on how to choose the appropriate operational amplifier with the focus on precision operational amplifiers with low offset voltage, bias current and noise as well as high slew rates. In this case the circuit was built with easily available operational amplifiers just to determine if the functionality was in line with what was desired. In the DAC8812 datasheet there are also guidelines on the layout of the circuit, including power capacitors on all of the voltage rails. Ideally the circuit should be constructed as compactly and cleanly as possible to avoid stray currents and voltages that may affect the output of the DAC. When the circuit is properly

implemented, these guidelines would all be closely followed to produce the best possible response with the lowest noise.

It is necessary to consider the margin for error in the DAC8812 by analysing the datasheet [24]. For the tested DAC8812, the typical full scale gain error corresponds to approximately 5 LSB, the maximum differential nonlinearity to 1 LSB and the maximum integral nonlinearity to 2 LSB. This leads to a potential error of approximately ±3 LSB. For a 10 V reference signal this corresponds to almost 0.1 μA current [29]. This is a large margin for error in an application that requires small current ranges. One way to improve this is to use a 5 V reference signal since a full scale output of 2 mA is higher than required and can be dropped without causing any problems. For a 5 V reference, the minimum output current increment of the DAC is 15 nA with a potential error of under 50 nA. This value can be lowered further by dropping the full scale output of the programmable current source through adjustments to the resistor values in the improved Howland Current Pump. Overall the DAC8812 with improved Howland Current Pump appears to be a suitable option to provide the bias current and flux modulation current.

Since the Digital Phase Splitter in Section 3.3.2 produces output voltages that switch between 0 and 5 V and not -5 and 5 V, some signal manipulation is required between the Digital Phase Splitter and DAC8812. This can easily be implemented with two operational amplifier stages. The first stage would be an inverting operational amplifier circuit with a gain of 2. This would change an output of the Digital Phase Splitter to switch between -10 V and 0 V. The second stage would be a simple inverting summing amplifier that adds 5 V (from the regulated voltage supply) to the output of the first stage. The output of the second operational amplifier would then switch between -5 V and 5 V as desired.

The programmable current source configuration can also be used to provide the necessary current to apply a flux offset to the SQUID. In this case, a constant 5 V reference could be used instead of the square-wave reference since no modulation is required. The flux modulation and flux offset currents would be connected to the feedback coil of the SQUID, while the bias current would be connected to the SQUID itself.

3.4 Lock-in Detection

Lock-in detection is required to extract the signal of interest from the modulated SQUID output. This is implemented by synchronously detecting the output voltage at the lock-in detection frequency.

This was considered in [30] for the design of a FLL using sinusoidal flux modulation. It was implemented using two analog Complementary Metal-Oxide-Semiconductor (CMOS) switches. The control signal for the first switch was obtained by passing the sinusoidal reference signal through an inverting comparator. The control signal for the second switch was obtained by passing the reference signal through a non-inverting comparator. Both of the comparators were operated as zero-crossing detectors with the second input connected to ground. The output of these comparators was then a square-wave signal. The input of the first switch was connected to the normal output of the amplification stage. The input of the second switch was connected to the the output of the amplification stage after it had been inverted. The outputs of both switches were connected together to produce a fully rectified output signal extracted from the flux modulated input.

A similar method is implemented in this research that caters for both bias current reversal and

flux modulation. As such, the control signals need to be produced from a reference signal with frequency and phase derived from the product of the bias reversal and flux modulation signals. Additionally, since square wave modulation is used, comparators are not required to produce the control signals for the switches. Figure 3.14 shows the circuit used to implement lock-in detection.

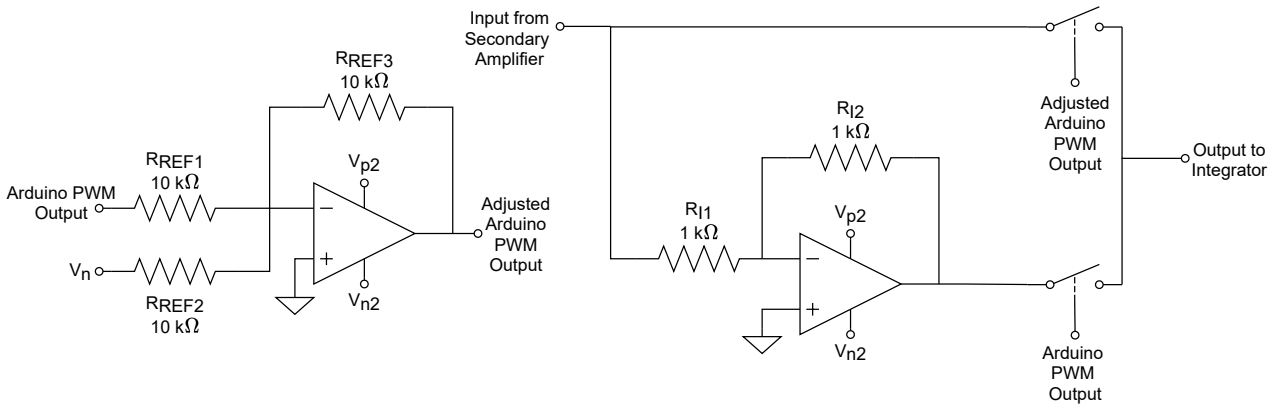


Figure 3.14: Diagram of the circuit configuration used for lock-in detection including necessary processing of Arduino PWM output signal.

The ADG1201 CMOS Single Pole Single Throw (SPST) switches from Analog Devices are chosen for their low leakage currents and fast switching times [31]. These switches require a minimum digital voltage of 2 V to close, and a maximum digital voltage of 0.8 V to open. Square-wave signals that switch between 0 V and 5 V are suitable for use as control signals.

For lock-in detection, each switch requires a different control signal. The control signal for the first switch should have the same frequency and phase as the reference signal (product of the bias current reversal and flux modulation signals). The control signal for the second switch should have the same frequency, but a phase-shift of 180°. The Arduino PWM output has the correct frequency and voltage output and is phase shifted by 180° from the reference signal. This makes it suitable for use as the second switch's control signal without any additional processing required. To obtain the control signal for the first switch the Arduino PWM output can still be used with some additional processing. This can be achieved by summing the Arduino PWM Output and -5 V from the regulated voltage supply and inverting the result. An inverting summing operational amplifier circuit is suitable for this. The circuit used to implement this is shown on the left-hand side of Figure 3.14.

The pre-amplifier and secondary amplification stages discussed in Chapter 4 produce an amplified output signal that is in-phase with the input signal from the SQUID. As such, it is also in phase with the reference signal. The output of the amplifying stages can be directly connected to the input of the switch that uses the processed Arduino PWM output for a control signal. For the switch that directly uses the Arduino PWM output, the output of the amplifying stage has to be inverted. This can be implemented using a simple inverting operational amplifier circuit with a gain of 1.

One issue with using the inverting operational amplifier circuit is the effect of the voltage offset on the output of the lock-in detection stage. This offset can cause a mismatch in the outputs of the two switches so that they don't align exactly and the measured output is not smooth. Choosing an operational amplifier with low voltage offset is extremely important as a result.

The LT1007 has very low noise and a low offset voltage of 25 μV making it suitable for this application [32].

Figure 3.15 shows the two control signals used for the switches. One signal is obtained directly from the Arduino and the other signal is processed through the inverting summing amplifier. Figure 3.16 shows how a modulated signal is obtained from an input signal. A simple triangular wave is modulated by a reference signal obtained from the product of the bias current reversal and flux modulation signals. The modulation of the SQUID is somewhat more complicated due to the sinusoidal response and four working points, but the principle of lock-in detection is the same.

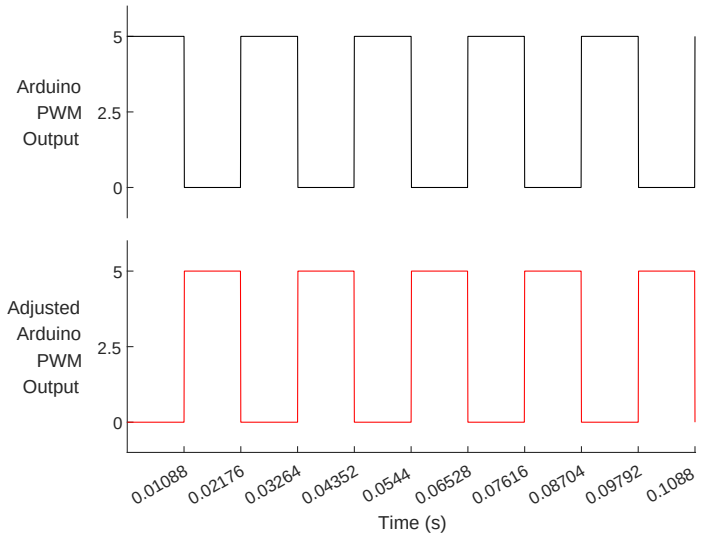


Figure 3.15: Theoretical control signals for the SPST switches used in lock-in detection.

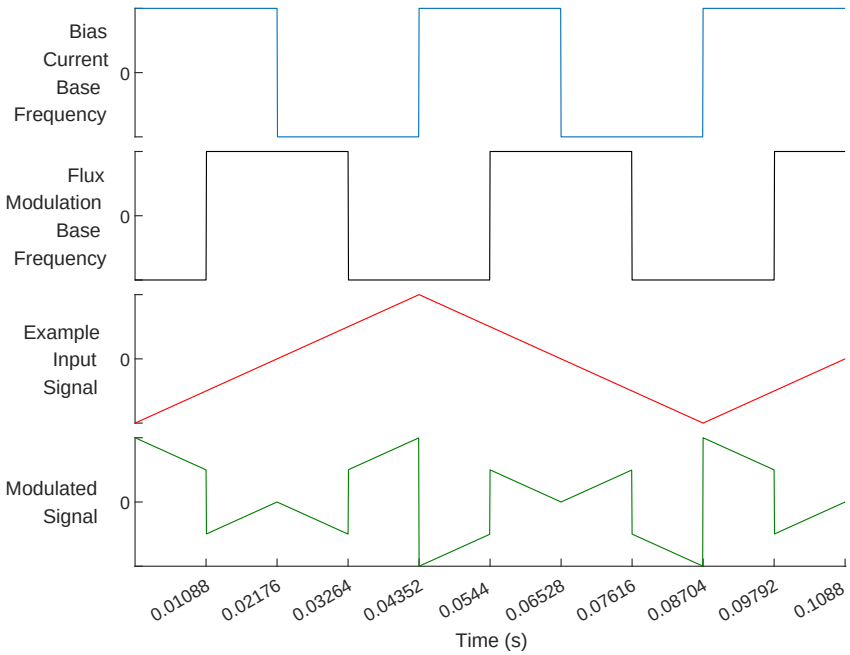


Figure 3.16: Theoretical example of a modulated signal using the bias current reversal and flux modulation signals from Section 3.3.2.

Figure 3.17 shows how the original signal is extracted from the modulated signal using the lock-in detection circuit in Figure 3.14. The modulated signal represents the normal output of the amplification stages (see Chapter 4) which is connected to the input of SPST 1. The control signal for SPST 1 is obtained from the adjusted Arduino PWM output. The inverted modulated signal is connected to the input of SPST 2 which obtains its control signal from the normal Arduino PWM output. When the switches see a control voltage of 0 V, they are open and there is no output. When they see a control voltage of 5 V, the switches are closed and the output is equal to the input. The summed output shows the result when the outputs of the two switches are connected together. It matches the original signal before modulation from Figure 3.16.

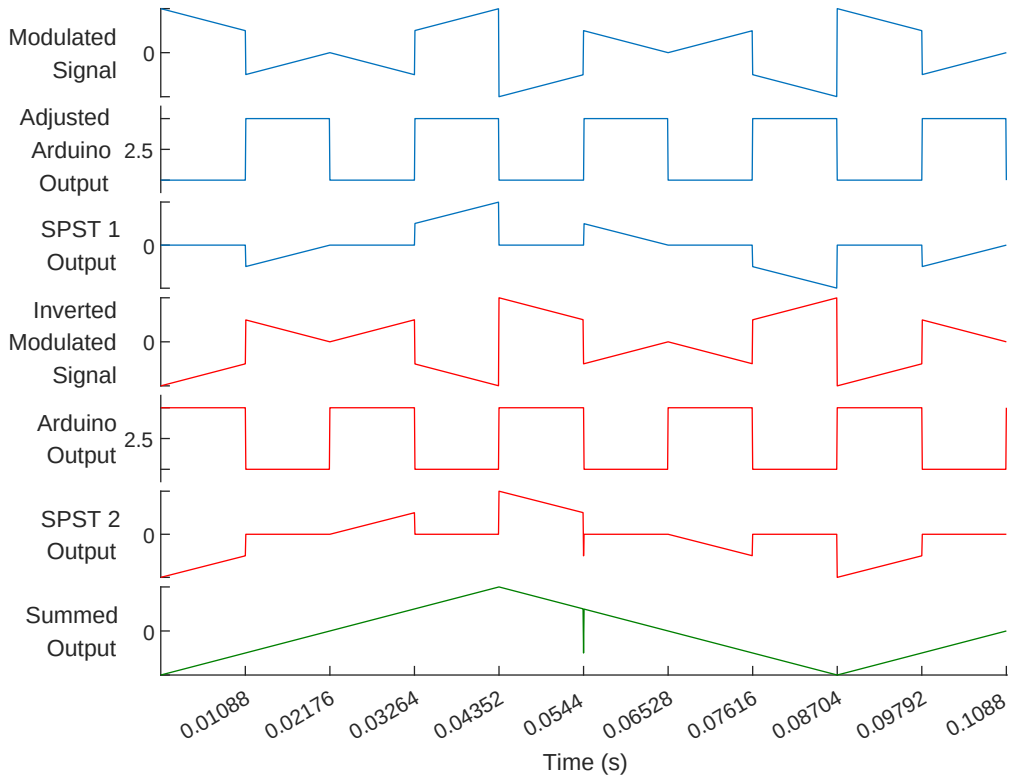


Figure 3.17: A theoretical representation of the extraction of the example input signal in Figure 3.16 from the modulated signal through lock-in detection.

3.5 Integration and Feedback

Both open-loop and closed-loop operation of a FLL is necessary for a SQUID measurement system. When a FLL is in open-loop configuration, the feedback resistor is connected to ground instead of the feedback coil. In this state, the system can be precisely tuned to the SQUID magnetometer being used.

To tune a SQUID, a test input signal is applied to the modulation coil in the form of a current. This signal is usually chosen as a triangular waveform with a peak-to-peak magnitude corresponding to $1\Phi_0$. This value is initially determined from the $1/M_f$ value given in a SQUID datasheet. For the M2700, a peak-to-peak current of 17 μA is required. The bias current, flux modulation current and flux offset current discussed in Section 3.3 can then be adjusted to obtain the maximum voltage output swing across the feedback resistor. Thereafter the test input signal can be adjusted to correspond exactly to $1\Phi_0$ (determined by the shape of the

output signal). This is the process used to tune a SQUID in [3].

Once the system has been tuned to the SQUID being used, it can be locked (switched to closed-loop operation). This is done by connecting the feedback resistor to the feedback coil instead of ground.

The integration and feedback system of the FLL is crucial to the tuning and locking of the FLL. It also determines the system's sensitivity to magnetic fields. Figure 3.18 shows the circuit diagram for the proposed integration and feedback system. This was based on the integrator system used in [33].

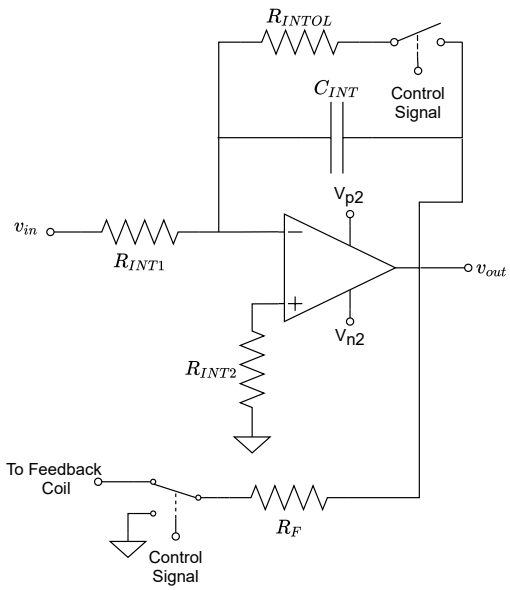


Figure 3.18: Circuit diagram of the integrator and feedback system of the FLL.

When the system is in open-loop configuration, the Single Pole Dual Throw (SPDT) switch after the feedback resistor is connected to the grounded output. Additionally a feedback resistor is connected in parallel with the integrator capacitor. This feedback resistor is chosen to limit the gain of the open-loop response of the FLL so that it falls within the the ± 10 V range chosen for the output. The resistors in the integrator are chosen as

$$R_{INT1} = R_{INT2} = R_{INTOL}$$

This limits the integrator to unity gain.

When the system is in closed-loop configuration, the SPDT switch after the feedback resistor is connected to the feedback coil output. Additionally a switch in series with the integrator feedback resistor is opened so that the gain is not limited and the integrator functions properly for closed-loop operation.

The feedback resistor R_F and the feedback mutual inductance $1/M_f$ determine the sensitivity of the SQUID (i.e the range of magnetic fields changes that can be measured). The calibration factor V_{Φ_0} in V/Φ_0 can be calculated as

$$V_{\Phi_0} = \frac{R_F}{M_f} \tag{3.3}$$

Given that the voltage output range at the integrator is chosen as ± 10 V, the full-scale output

of the FLL in terms of Φ_0 can be determined from

$$FS = \frac{20V}{V_{\Phi_0}} \tag{3.4}$$

For the M2700, feedback resistor values of 600 kΩ, 60 kΩ and 6 kΩ were chosen with $1/M_f = 17\ \mu A/\Phi_0$. This results in calibration factors of 10.2 V/Φ_0, 1.02 V/Φ_0 and 102 mV/Φ_0 and full-scale ranges of $1.96\Phi_0$, $19.6\Phi_0$ and $196\Phi_0$ respectively.

The time constant of the integrator is a contributing factor in determining the closed loop bandwidth (f_{-3dB}) of the system (discussed further in Chapter 5). The larger the time constant, the smaller the bandwidth. With the calibration factor changing for different sensitivities, the time constant also has to change to keep the system bandwidth constant [33]. Initially, integrator capacitor and resistor values were chosen to produce time constants in the same order as those from [3]. They were chosen slightly larger since this research was focused on low frequency measurements and large bandwidths were not necessary. Time constants of 20 μs, 200 μs and 2 ms were chosen. With $R_{INT1} = 10$ kΩ this leads to capacitor values of 2 nF, 20 nF and 200 nF respectively.

Table 3.3 contains a summary of the initial values for the capacitors and resistors used in the integration and feedback stage with corresponding time constants, calibration factors and full-scale range.

Table 3.3: Summary of the initial values for the integration and feedback stage with corresponding time constants, calibration factors and full-scale range

Feedback Resistor	Calibration Factor	Full-scale Range	Integration Time	Integrator Capacitor	Integrator Resistor
600 kΩ	10.2 V/Φ_0	$1.96\Phi_0$	20 μs	2 nF	
60 kΩ	1.02 V/Φ_0	$19.6\Phi_0$	200 μs	20 nF	10 kΩ
6 kΩ	102 mV/Φ_0	$196\Phi_0$	2 ms	200 nF	

The operational amplifier used for the integrator still needs to conform to low noise requirements, but also has to be a high-speed component with a large slew rate. The LT1028 operational amplifier from Analog Devices is chosen as being suitable for this application with its minimum slew rate of 11 V/μs [34]. The same SPST switch used for lock-in detection (ADG1201) can be used for the switch connected to the integrator's feedback resistor [31]. The ADG1219 from Analog Devices can be used as the SPDT switch used to change between open-loop and closed-loop FLL operation. For this switch, high-speed switching it not important so the focus is on a low current leakage [35]. Both the SPDT and SPST can be controlled from a digital pin on a microcontroller.

3.6 Microcontroller and Software

It is important to choose the right microcontroller with all of the required functionality for controlling the FLL. The development boards produced by Arduino are a very suitable option. They have a wide range of functionality, easy to use hardware, well-documented software libraries and are relatively inexpensive. Arduino has its own programming language, but it is also possible to use an Arduino with Python. This is desirable since user interfaces can easily be developed using Python.

The Arduino Mega 2560 Rev3 is best suited to this application due to the simple USB interface with a PC and the high number of digital input/output pins available. Since the FLL has a large number of adjustable parameters and multiple current sources that need to be controlled using SPI, a large number of pins is required. The Arduino Mega also has the required 16 bit timers to produce the PWM output signal used for modulation and lock-in detection [36].

Figures 3.19, 3.20 and 3.21 show the screen design of a very simple user interface created using Qt for Python. The screen designs were based on the functionality for the proposed FLL design in this research and the functionality of the software developed by Star Cryoelectronics and Magnicon for FLL control [3] [4].

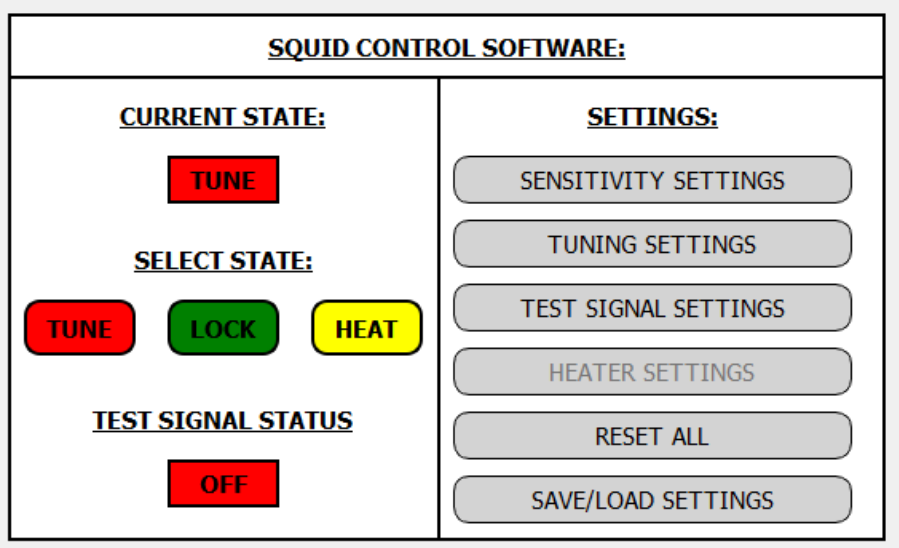


Figure 3.19: Example of the main screen for a simple user interface to control the SQUID FLL. Generated using Qt for Python.

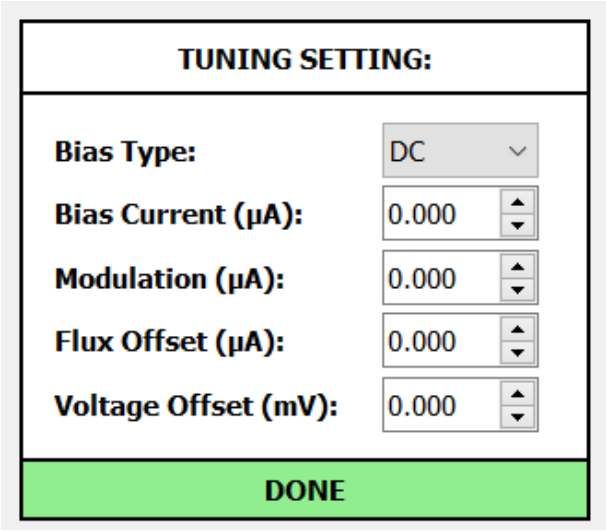


Figure 3.20: Example of the tuning setting screen for a simple user interface to control the SQUID FLL. Generated using Qt for Python.

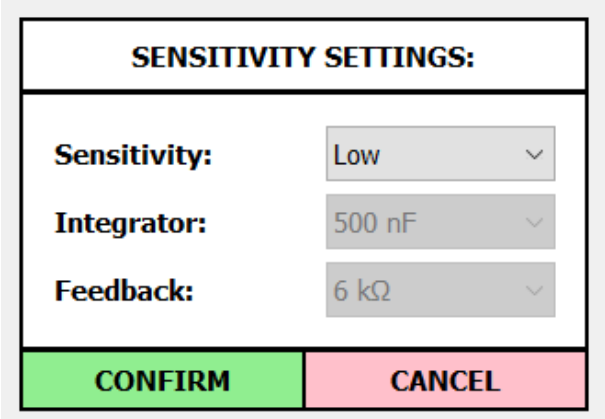


Figure 3.21: Example of the sensitivity settings for a simple user interface to control the SQUID FLL. Generated using Qt for Python.

Chapter 4

Low Noise Amplifier

Possibly the most important part of a Flux-Locked-Loop is the initial low noise pre-amplifier. If the noise contribution of the the amplification stages is higher than the noise floor of the SQUID, the range of magnetic field changes that the SQUID can measure is limited by the amplification stages.

This chapter discusses the concept of noise and the dominant noise sources present in a circuit. It also considers two types of input stage for a pre-amplifier: common emitter amplifiers and differential amplifiers. The final design choice is presented and subsequent amplification stages that remove the offset voltage of the SQUID are discussed.

4.1 Noise

In [14], noise is defined as "any unwanted disturbance that obscures or interferes with a desired signal". Noise is of vital importance in sensor measurement systems, since it is often the limiting factor that determines the smallest measurement that can be made.

Types of Noise

There are three dominant types of noise in a circuit: thermal noise, shot noise and flicker ($1/f$) noise.

Thermal noise (otherwise known as Johnson or Nyquist noise) is noise due to current fluctuations caused by the random movement of electrons in conductors. These current fluctuations give rise to a voltage across the conductor that is dependent on the temperature of the conductor and its resistance [14]. Reactive components do not contribute any thermal noise. Thermal noise contributes to the flatband noise of a circuit. The RMS thermal noise voltage of a resistor is calculated as

$$E_{RMS} = \sqrt{4kTR\Delta f} \quad V_{RMS} \tag{4.1}$$

where k is Boltzmann's constant ($k = 1.38 \times 10^{-23}\text{J.K}^{-1}$), T is the temperature of the conductor in Kelvin, R is the resistance and Δf is the noise bandwidth. This can also be written as a noise current

$$I_{RMS} = \sqrt{\frac{4kT\Delta f}{R}} \quad V_{RMS} \tag{4.2}$$

When determining the noise response of a circuit, it is preferred to work with noise in terms of the RMS voltage in 1 Hz of noise bandwidth (in $V/\sqrt{\text{Hz}}$). This is calculated as

$$E_R = \frac{E_{RMS}}{\sqrt{\Delta f}} = \sqrt{4kTR} \quad V/\sqrt{\text{Hz}} \tag{4.3}$$

Shot noise is noise resulting from fluctuations in the flow of current across a potential barrier such as a pn junction [14]. These fluctuations are a result of the small current pulses produced by electrons crossing the potential barrier. Shot noise is calculated as

$$I_s = \sqrt{2qI_{DC}} \quad V/\sqrt{\text{Hz}} \tag{4.4}$$

where q is the charge on an electron (1.602×10^{-19} C) and I_{DC} is the DC current flowing across the junction. Since this noise requires a potential barrier, it is not present in resistors. Like thermal noise, shot noise contributes to the flatband noise of a circuit.

Flicker noise, also known as low frequency and $1/f$ noise, is noise that increases with decreasing frequency. The spectral density of this noise generally conforms to a $1/f$ characteristic where spectral density is $S(f) = \frac{E^2_{RMS}}{\Delta f}$. In [14], this noise is attributed to properties of the semiconductor's surface and the resulting interactions of charge carriers with the surface. Flicker noise is of great concern in this research due to the focus on low frequency measurements.

Figure 4.1 shows a typical plot of noise voltage density against frequency. The $1/f$ corner frequency (f_C or f_L) is very important since it provides an indication of the crossover point between $1/f$ noise and flatband noise.

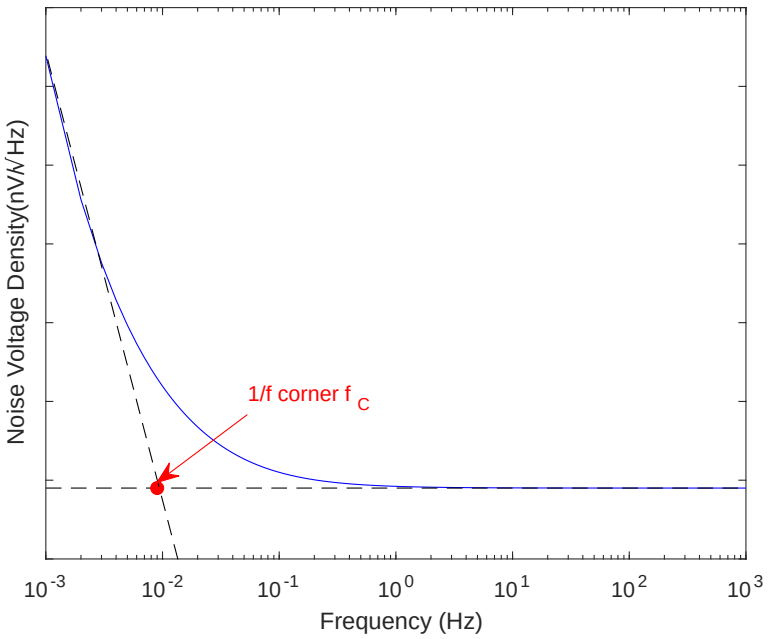


Figure 4.1: Example plot of noise voltage density against frequency.

Noise Bandwidth:

The noise bandwidth (Δf) discussed above is not the same as the system bandwidth f_{-3dB}. Noise bandwidth of a system can be determined from a plot of the squared voltage gain against

frequency. Dividing the integral of this curve by the squared maximum gain of the system gives the noise bandwidth [14]. This calculation is often difficult to make for more complicated circuits. In [1], it is mentioned that for a FLL with a first-order low-pass response, the noise bandwidth can be approximated by multiplying the system bandwidth f_{-3dB} by $\pi/2$. This approximation is used for the FLL design under consideration.

Equivalent Input/Output Noise:

When noise analysis is performed for a circuit, the aim is typically to determine the equivalent input or output noise of the circuit. To do this, the thermal, shot and flicker noise contribution needs to be considered for every component at the circuit's input or output. The equivalent input or output noise is then the total noise contribution at the input or output. When considering noise sources, the total contribution of uncorrelated noise sources is determined by RMS summing the individual sources:

$$E_{tot}^2 + E_1^2 + E_2^2 \tag{4.5}$$

Correlated noise sources are not considered in this research.

To determine the noise contribution of each noise source, a circuit diagram should be drawn that includes all noise sources as voltage or current sources. For thermal noise sources, a noise voltage is in series with the resistor and a noise current is in parallel with the resistor.

Since all noise sources are uncorrelated, the principle of superposition can be used to simplify the noise analysis of the circuit by considering the noise contribution of each source separately. Basic circuit analysis techniques can be used to determine the contribution of the noise source as if it was a normal voltage or current source with one small difference: since noise sources are RMS summed, the gain of the noise contribution to the input or output must be squared. For example, if the contribution of a voltage source at the output is $V_{out} = KV_1$ then the contribution of a voltage noise source to the output noise would be $E_{out}^2 = K^2E_1^2$. As a result, noise sources are always added together since the individual noise contributions will always be positive.

If the equivalent output noise is calculated, the equivalent input noise can be determined by dividing this value by the squared gain of the circuit from input to output.

One useful attribute of resistor noise is related to parallel resistors. The noise response of resistors in parallel is the same as the noise response of a single resistor with resistance equal to the resistance of the parallel pair.

$$E_{R_1}^2 + E_{R_2}^2 = E_{R_1||R_2}^2 = \frac{4kT}{R_1||R_2} \tag{4.6}$$

Input Devices

Motchenbacher and Conelly [14] provide a guide to choosing the most suitable input device for a low noise amplifier according to the source resistance seen by the amplifier. In the case of the M2700, the source resistance is either 5 Ω without the transformer or 125 Ω with the transformer. These are very low values of source resistance so Bipolar Junction Transistors (BJTs) are the most suitable for the amplifier input stage. They have lower voltage noise and higher current noise relative to other options such as JFETs or MOSFETS [14]. For higher source resistance applications, the high current noise would have a large impact on the total noise of the circuit.

For low source resistance applications, the impact of current noise is minimised and the voltage noise of the input device is of larger concern. As such, a BJT input stage is the most suitable for the FLL design.

A BJT transistor has four dominant noise sources: thermal noise from the base-spreading resistance r_x, shot noise generated by the collector current I_C, shot noise generated by the base current I_B and flicker noise due to the base current flowing through the base-emitter depletion region [14]. The formulae for these noise sources are

$$E_{rx}^2 = 4kTr_x \tag{4.7}$$

$$I_{sic}^2 = 2qI_C \tag{4.8}$$

$$I_{sib}^2 = 2qI_B \tag{4.9}$$

$$I_{fib}^2 = \frac{2qf_L I_B^\gamma}{f} \tag{4.10}$$

Variable γ in equation (4.10) is known as the flicker noise exponent. The value of γ can range from 1 to 2, but is assumed to be 1 for typical $1/f$ noise [37]. The term $2qf_L$ is known as the flicker noise coefficient where f_L is taken as the corner frequency of the transistor [38].

From the equation for flicker noise, it is clear that large I_B values lead to increased flicker noise in the transistor. On the other hand, the shot noise contribution of I_C at the input of the transistor decreases with increasing collector current since

$$\frac{2qI_C r_\pi^2}{\beta^2} = \frac{2qV_T^2}{I_C} \tag{4.11}$$

This noise contributes to the flatband noise of the transistor. As a result, it is necessary to find a balance between flicker noise and flatband noise by carefully selecting the I_C value for a BJT.

Some transistor datasheets supply noise information in the form of voltage noise (E_n) and current noise (I_n). This removes the need to calculate each individual noise source for the transistor. Other datasheets provide very little or no noise information which makes flicker noise calculations inaccurate since f_L has to be estimated.

Horrowitz and Winfield [12] provide detailed tables of the noise characteristics for discrete low noise BJTs and matched pair BJTs. These tables are used in Sections 4.2 and 4.3 to select appropriate transistors.

Noise Simulation in LTspice

LTspice XVII can be used to perform noise analysis. It provides functionality for plotting the equivalent input and output noise voltage densities against frequency for a circuit where the input and output nodes are specified. Additionally, the noise contribution of every noise source as seen at the output, can be plotted individually. A plot of circuit gain from input to output against frequency can also be obtained.

For a BJT, LTspice calculates 6 different noise contributions: the thermal noise of r_x (called R_B in the BJT model), the thermal noise of the collector and emitter resistors (R_C and R_E in the BJT model), the shot noise of I_B and I_C and the flicker noise due to I_B. The thermal noise contribution of R_C and R_E is normally very small when compared with other noise contributions and is ignored in calculations.

Figure 4.2 shows the LTspice noise model of a BJT.

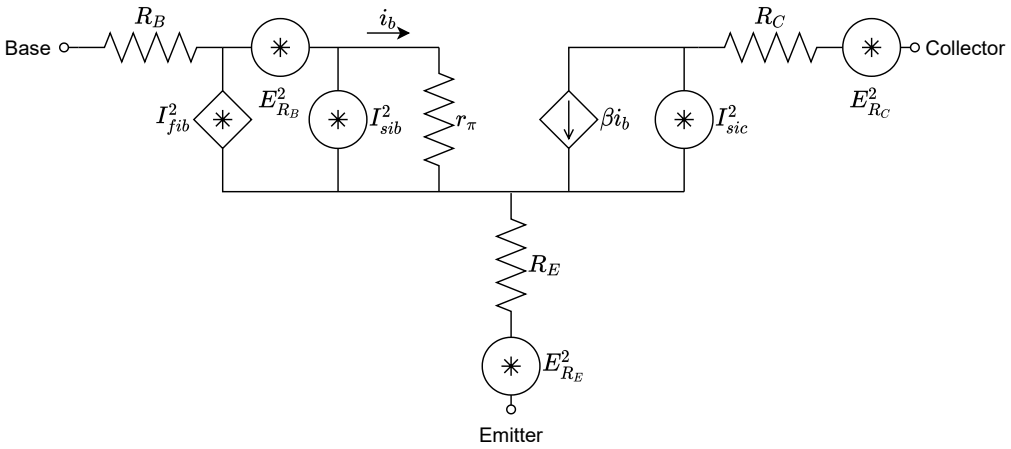


Figure 4.2: LTspice noise model of a BJT transistor.

The BJT model for a transistor includes two parameters that are required to calculate the flicker noise. AF in the model corresponds with the flicker noise exponent γ and KF corresponds with the flicker noise coefficient $2qf_L$ [38]. AF is assumed to be 1 throughout this research.

LTspice also provides functionality to integrate the noise voltage density curve over a specified noise bandwidth. This can be used to determine the total RMS noise contribution of the circuit in V_{RMS}.

For LTspice, thermal noise contributions assume a room temperature of T = 300 K. This value is used for all hand calculations in this chapter so that the results can be directly compared with LTspice simulation results.

4.2 Common Emitter Amplifier

The first Low Noise Amplifier (LNA) design that was considered uses a common emitter input stage. Common emitter amplifiers are capable of achieving large voltage gains. This is desirable since the gain of a pre-amplifier input stage attenuates the noise contributions of subsequent secondary amplification stages. At the time that the common emitter amplifier was designed, information on the actual source resistance of the considered SQUID (M2700) was not available. Using [39] as a basis, a source resistance less than 100 Ω was assumed.

The table of low noise BJTs in [12] was used to select suitable transistors for the design. BJTs with low β and V_A values were disregarded due to the high gain requirement. Additionally, transistors whose optimum source resistance was larger that 200 Ω were ignored due to the assumed low source resistance from the SQUID. The list was then narrowed down further according to the best noise characteristics and availability from electronics suppliers. The final shortlist consisted of the 2SA1312 pnp BJT from Toshiba [40] and the DSS20201L and ZXTN19100CFF npn BJTs from Diodes Incorporated [41] [42].

Figures 4.3 and 4.4 on the next page show the circuit configurations for the npn and pnp transistors respectively. R_S is the source resistance (i.e. the resistance of the SQUID as seen by the circuit). This design uses the +5 V and -5 V regulated voltages supplies discussed in Section 3.2. The bypass capacitor C_E is utilised to ensure that the amplifier can achieve the

high gain that is desired. It has an added benefit of attenuating the noise contribution of the emitter resistor.

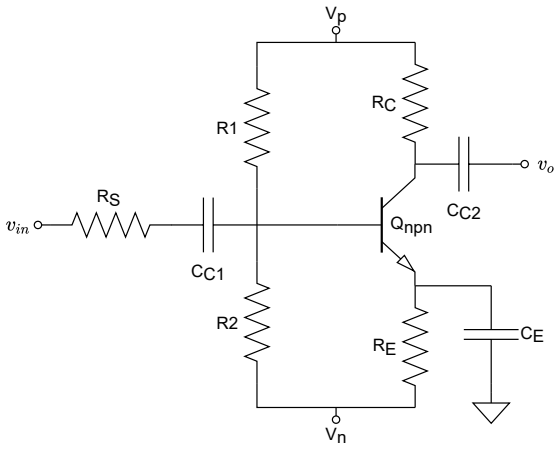


Figure 4.3: Common emitter configuration for a npn BJT.

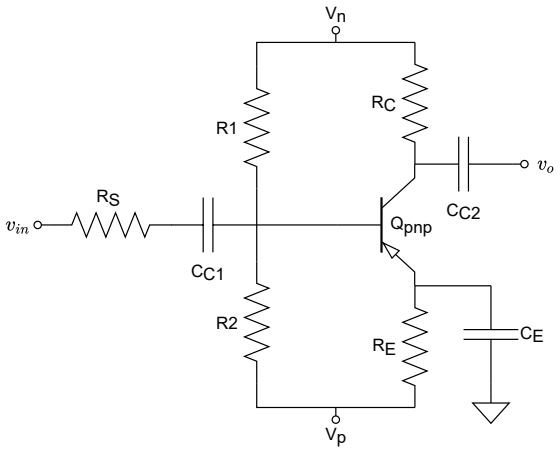


Figure 4.4: Common emitter configuration for a pnp BJT.

4.2.1 Circuit Analysis

The design process for the npn and pnp transistors is the same, so only the npn method is shown here. This process uses concepts from [43]. Secondary amplification would be implemented using operational amplifiers with large input impedance. Therefore the loading effect of secondary stages is ignored in the design process.

Figure 4.5 shows the small signal equivalent circuit for the npn common emitter amplifier.

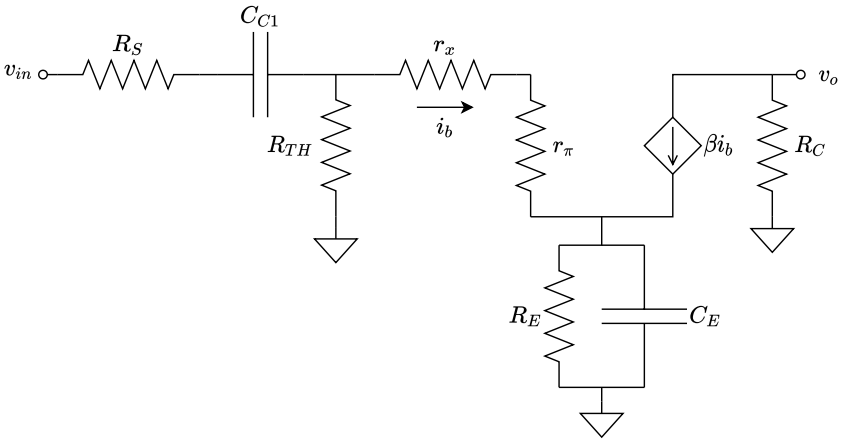


Figure 4.5: Common emitter small signal equivalent circuit for a npn BJT.

Assumptions:

$$V_{BE(on)} = V_{EB(on)} = 0.7V$$
$$V_{CE(sat)} = V_{EC(sat)} = 0.2V$$

' The current relationships in the BJT are

$$I_C = \beta I_B \tag{4.12}$$

$$I_E = (\beta + 1)I_B \tag{4.13}$$

It is assumed that R_S is small relative to $R_{TH}||r_\pi$ where $R_{TH} = R_1||R_2$. The gain of the circuit is then calculated as

$$A_V \approx \frac{-\beta R_C}{r_\pi + r_x} \tag{4.14}$$

For optimal output swing, the following should hold true

$$R_{DC} = R_C + R_E \tag{4.15}$$

$$R_{AC} = R_C \tag{4.16}$$

$$R_{DC} + R_{AC} = \frac{V_p - V_{CE(sat)} - V_n}{I_C} \tag{4.17}$$

From the formulae for gain and optimal output swing, the resistances R_C and R_E can be calculated.

$$R_C = A_V(\frac{V_T}{I_C} + \frac{r_x}{\beta}) \approx A_V\frac{V_T}{I_C} \tag{4.18}$$

$$R_E = \frac{V_p - V_{CE(sat)} - V_n}{I_C} - 2R_C \tag{4.19}$$

For bias stability we use the following equation

$$R_{TH} = 0.1\beta R_E \tag{4.20}$$

And so R_1 and R_2 can be calculated as

$$R_1 = \frac{R_{TH}(V_p - V_n)}{I_B R_{TH} + V_{BE(on)} + I_E R_E} \tag{4.21}$$

$$R_2 = \frac{R_{TH}R_1}{R_1 - R_{TH}} \tag{4.22}$$

A large gain of A_V = -180 was chosen for the common emitter amplifier. Circuits using the three transistors under investigation were then designed for a range of collector currents between 1 and 100 mA. Random large capacitors were used at this stage, with final values to be selected during noise analysis.

The BJT Spice models for each of the transistors was obtained from the supplier websites. The designs were then simulated in LTspice (without any-fine tuning) to determine the base noise, gain and bandwidth for each design. From these simulations, eight designs were selected for further simulation and testing. These designs included the 2SA1312 for I_C = 1 mA, 5 mA and 10 mA, the DSS20201L for I_C = 1 mA, 5 mA and 10 mA and the ZXTN19100CFF for I_C = 5 mA and 10 mA. The ZXTN19100CFF showed poor performance at I_C = 1 mA which was why it was only considered for I_C = 5 mA and 10 mA.

4.2.2 Noise Analysis

Figure 4.6 on the next page shows the small signal equivalent circuit for the npn common emitter amplifier including all noise sources. The only difference for the equivalent circuit using a pnp transistor is that the current directions of i_b and βi_b are reversed. The noise calculations are identical for npn and pnp transistors.

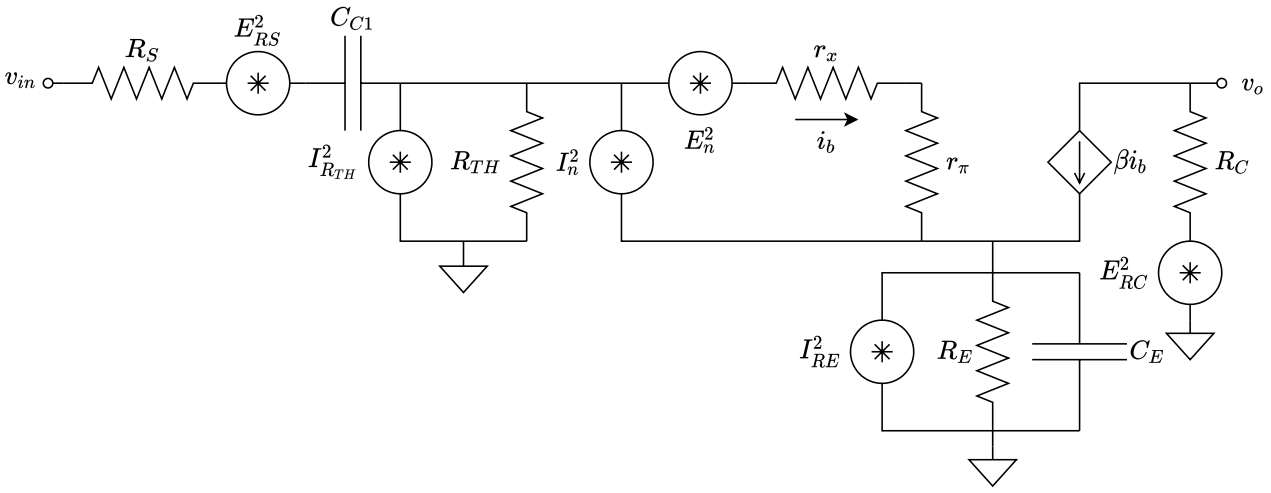


Figure 4.6: Common emitter small signal equivalent circuit for a npn BJT including noise sources.

The noise effect of subsequent operational amplifier amplification stages was assumed to be negligible, since any noise would be attenuated by the large gain of the common emitter stage. This was an incorrect assumption since it did not consider how much the flicker noise contribution of the operational amplifier's current noise could affect the system noise. This is discussed further in Section 4.2.5.

Since the voltage and current noise flatband values (E_n and I_n) were available in [12] for the BJT transistors under consideration, explicit calculation of each transistor noise contribution was not implemented. As a result, the equivalent input noise calculations in this section only considered the flatband noise without including the effect of flicker noise. It was assumed that the LTspice BJT models accounted for flicker noise and that the noise simulation results reflected that. This was determined to be incorrect at a later stage and is discussed further in Section 4.2.5.

The method and equations for noise analysis in this section are based on an example of a common emitter amplifier in [14]. These noise calculations are used to determine the appropriate capacitor values for the circuit.

Equations (4.23)-(4.26) calculate the base value of each thermal noise source in the circuit.

$$E^2_{RC} = 4kTR_C \tag{4.23}$$

$$E^2_{RE} = 4kTR_E = I^2_{RE}R^2_E \tag{4.24}$$

$$E^2_{RS} = 4kTR_S \tag{4.25}$$

$$I^2_{RTH} = \frac{4kT}{R_{TH}} \tag{4.26}$$

A few assumptions are made to simplify the noise analysis. It is assumed that the source resistance is small and that the loading of the secondary amplification is large. Thus we have

$$(R_S + \frac{1}{j\omega C_{C1}})||R_{TH}||(r_x + r_\pi + (\beta+1)R_E||\frac{1}{j\omega C_E}) \approx (R_S + \frac{1}{j\omega C_{C1}}) \tag{4.27}$$

The noise contribution of the collector resistor R_C at the input is found by dividing the noise

source by the square of the circuit gain.

$$E_{iRC}^2 = (\frac{1}{A_V})^2 E_{RC}^2 \tag{4.28}$$

Noise from the emitter resistor would normally be directly added to the input noise of the circuit, however, the bypass capacitor C_E attenuates this noise contribution [14].

$$I_{RE}^2 \left|(R_E||C_E)\right|^2 = \frac{I_{RE}^2 R_E^2}{1+(\omega R_E C_E)^2} = \frac{E_{RE}^2}{1+(\omega R_E C_E)^2} \tag{4.29}$$

The formula for the equivalent input noise of the amplifier is then

$$\begin{aligned} E_{ni}^2 = E_{RS}^2 \ + \ (I_{RTH}^2 + I_n^2)(|R_S + \frac{1}{j\omega C_{C1}}|)^2 \ + \ (\frac{R_S + R_{TH}}{R_{TH}})^2 E_n^2 \ + \ (\frac{1}{A_V})^2 E_{RC}^2 \\ + \ \frac{E_{RE}^2}{1+(\omega R_E C_E)^2} \end{aligned} \tag{4.30}$$

The effect of C_{C1} is ignored for the E_n noise contribution of the transistor for simplification purposes.

From this equation we can determine some appropriate design choices for C_{C1} and C_E. Since C_E attenuates the noise of the emitter resistor, a large value should be selected. Since $\frac{1}{C_{C1}}$ increases the noise contribution of I_n and I_{RTH}, a large value for C_{C1} is also desirable. C_{C2} is not shown in the diagram, but follows the same principal as C_{C1} where $\frac{1}{C_{C2}}$ increases the voltage noise contributions of secondary amplification stages.

Since the amplifier needs to be operate at sub 1 Hz frequencies, the low frequency cutoff due to the the three capacitors also needs to be taken into consideration. For each of the designs, the bypass capacitor sees the smallest equivalent resistance and has the largest effect on the overall cutoff frequency of the circuit. Both the noise analysis and frequency analysis require that this capacitor be extremely large. A supercapacitor with a value of 1 F was selected. A slightly smaller capacitor of 0.1 F was chosen for coupling capacitors C_{C1} and C_{C2}.

The choice of capacitor values introduced a major design flaw that is discussed in Section 4.2.5.

4.2.3 Simulation

The resistor values in the eight shortlisted designs were fine-tuned to obtain the best possible gain and output voltage swing. Standard resistor values that were close to these fine-tuned values were chosen. Table 4.1 on the next page shows the final component values for each design as well as the β value used in calculations. For simulation and testing, a large load of 100 kΩ was chosen to correspond to a high input resistance for secondary amplification stages. The source resistance was assumed to be 50 Ω to match with the output impedance of the signal generator that would be used for testing. Since the resistance of the SQUID was assumed to be under 100 Ω, this value was suitable.

Figures B.1, B.2 and B.3 in Appendix B show the magnitude of the gain and equivalent input noise for each I_C design as obtained by simulation for the 2SA1312, DSS20201L and ZXTN19100CFF BJTs respectively. Table 4.2 on the next page contains a summary of the simulation results for each of the eight designs.

Table 4.1: Component values used for simulation and testing of the common emitter amplifier.

	2SA1312			DSS20201L			ZXTN19100CFF	
	1 mA	**5 mA**	**10 mA**	**1 mA**	**5 mA**	**10 mA**	**5 mA**	**10 mA**
β	415			390			390	
$\mathbf{R_1}$	154 kΩ	30.9 kΩ	15.4 kΩ	145 kΩ	28.7 kΩ	14.3 kΩ	28.7 kΩ	14.5 kΩ
$\mathbf{R_2}$	21.24 kΩ	4.3 kΩ	2.15 kΩ	20 kΩ	4.02 kΩ	2 kΩ	4.02 kΩ	1.845 kΩ
$\mathbf{R_C}$	4.7 kΩ	931 Ω	470 Ω	4.7 kΩ	931 Ω	470 Ω	931 Ω	470 Ω
$\mathbf{R_E}$	549 Ω	105 Ω	50 Ω	549 Ω	105 Ω	50 Ω	105 Ω	44.2 Ω
$\mathbf{R_L}$	100 kΩ							
$\mathbf{R_S}$	50 Ω (Output Impedance of Signal Generator)							
$\mathbf{C_{C1}}$	0.1 F							
$\mathbf{C_{C2}}$	0.1 F							
$\mathbf{C_E}$	1 F							

Table 4.2: Summary of the simulation results for the eight common emitter circuit configurations under investigation.

	2SA1312			DSS20201L			ZXTN19100CFF	
	1 mA	**5 mA**	**10 mA**	**1 mA**	**5 mA**	**10 mA**	**5 mA**	**10 mA**
Flatband ($nV/\sqrt{Hz}$)	1.028	0.956	0.952	1.022	0.949	0.950	0.952	0.962
1 mHz Noise ($nV/\sqrt{Hz}$)	2.596	5.029	6.967	2.695	5.289	7.190	5.877	8.006
Gain at 5 Hz	166.08	149.25	133.20	170.64	169.79	163.51	163.84	151.03
Gain at 100 mHz	165.70	143.65	119.43	170.44	162.02	139.90	156.44	130.91

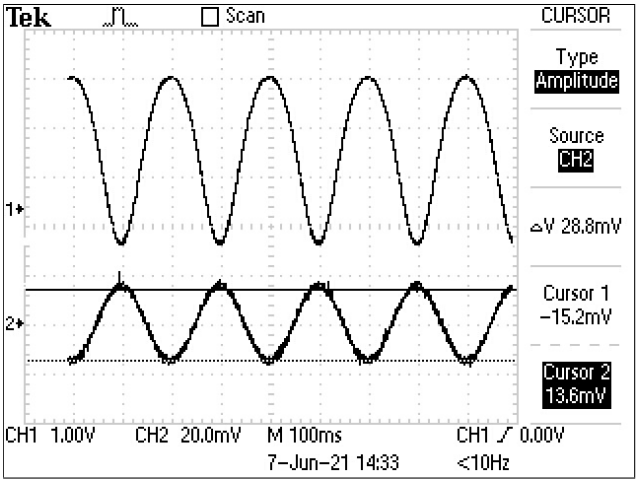
From the simulation results, it appears that the 5 mA DSS20201L design would be the most suitable. It maintained a good gain at both 5 Hz and 100 mHz, has low flatband noise and acceptable flicker noise (based on the noise measured at 1 mHz). It was only at a later stage that it was determined that this flicker noise value was very inaccurate. This is discussed further in Section 4.2.5.

4.2.4 Testing

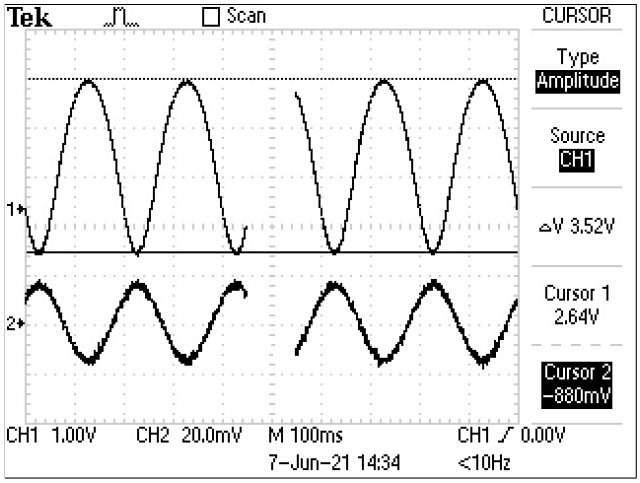
The eight common emitter amplifier designs were built and tested using a DC power supply, signal generator and oscilloscope. The signal generator was set to produce a sine wave with amplitude 15 mV (the lowest signal that the generator could provide) and frequencies of 5 Hz or 100 mHz. The output and input voltages were measured to determine the gain of the circuit at each of these two frequencies .

Figures C.1 to C.8 in Appendix C show the measured input and output voltages for each design at both 5 Hz and 100 mHz. Figure 4.7 on the next page shows a subsection of the measured results from Appendix C. Specifically, it shows the results for the DSS20201L BJT design at 1 mA.

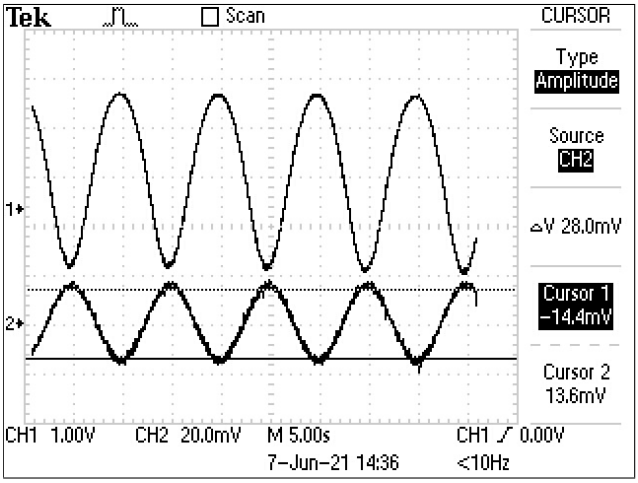
Table 4.3 on the next page contains a summary of all of the measured results with the calculated gain for each design.



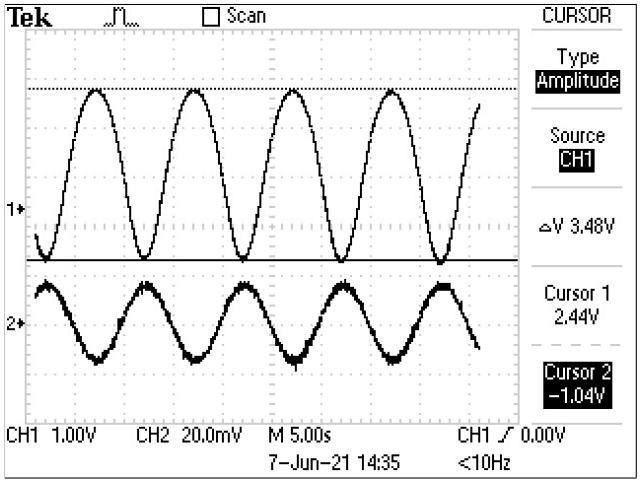
(a) Input at 5 Hz



(b) Output at 5 Hz



(c) Input at 100 mHz



(d) Output at 100 mHz

Figure 4.7: Measured results of the DSS20201L transistor at 1 mA.

Table 4.3: Summary of the oscilloscope measurements for the eight common emitter circuit configurations under investigation.

Measured I_{CQ}	Frequency	Input (mV)	Output (V)	Gain
2SA1312				
0.835 mA	5 Hz	-12.8 to 16	-2.64 to 0.72	116.67
	100 mHz	-12.8 to 15.2	-2.64 to 0.64	117.14
4.281 mA	5 Hz	-13.2 to 15.6	-2.32 to 0.72	105.56
	100 mHz	-13.6 to 14.8	-2.08 to 0.48	90.14
8.991 mA	5 Hz	-12.4 to 15.2	-1.6 to 0.92	91.30
	100 mHz	-14 to 15.2	-1.24 to 0.52	60.27
DSS2021L				
0.876 mA	5 Hz	-15.2 to 13.6	-0.88 to 2.64	122.22
	100 mHz	-14.4 to 13.6	-1.04 to 2.44	124.29
3.397 mA	5 Hz	-14.4 to 14.4	-1.36 to 1.96	115.28
	100 mHz	-14 to 15.2	-0.96 to 1.64	89.04
9.162 mA	5 Hz	-13.6 to 14.4	-1.12 to 1.64	98.57
	100 mHz	-12.8 to 14.4	-0.6 to 1.24	67.65

ZXTN19100CFF				
4.352 mA	5 Hz 100 mHz	-13.2 to 14.4 -14 to 14.8	-1.76 to 1.52 -1.48 to 1.12	118.84 90.28
9.258 mA	5 Hz 100 mHz	-13.6 to 14 -13.6 to 14	-0.76 to 1.84 -0.36 to 1.44	94.20 65.22

It is evident that the DSS20201L design for 1 mA is the most suitable of the eight designs since it provides the highest gain that is relatively consistent at 5 Hz and 100 mHz. The gain is considerably lower than the one obtained by simulation though. This is likely due to a difference in the β value of the actual transistor with the β value used for simulation and calculation.

For all of the amplifier designs, the output voltages appeared to swing unevenly without showing obvious signs of distortion. This was likely due to the fact that the circuits had not yet reached their steady state value when the measurements were taken. This is discussed further in the following section.

4.2.5 Design Flaws

While the common emitter amplifier initially seemed like a good design choice for the the pre-amplifier input stage, simulation and testing exposed a number of design flaws.

Flicker Noise

It was initially assumed that the transistor models included the necessary parameters to simulate the flicker noise of the BJT since simulation results appeared to present the expected $1/f$ noise response. On closer inspection, the transistor models did not include values for the flicker noise coefficient ($KF = 2qf_L$). When this value is not specified in the model, the default is set to 0 and no flicker noise component is calculated. The apparent $1/f$ noise response was due to the increased noise contribution of sources like E_{RC} as the gain of the circuit dropped for frequencies below the low cutoff point.

None of the three shortlisted transistor datasheets included information on the corner frequency of the transistor's noise. This information was also not found in the table of low noise BJTs in [12]. As such, a very low corner frequency of $f_L = 1$ Hz was chosen. This value is likely far lower than the actual corner frequency for the transistors, but was selected to give an optimistic idea of the flicker noise response in the circuit.

The circuit was simulated again with the flicker noise coefficient $KF = 2qf_L = 3.2 \times 10^{-19}$. Figure 4.8 on the next page shows the simulation results for the DSS20201L BJT at $I_C = 1$ mA. The simulated noise at 1 mHz is over 20 times higher than it was in the original simulation that didn't account for the transistor's flicker noise.

Another incorrect assumption was that the noise contributions of the secondary amplification stage could be ignored due to the high gain of the input stage. In the case of the flatband noise, this assumption holds true. When considering the flicker noise contribution of the operational amplifier, however, the results are completely different.

The circuit was simulated again with added secondary amplification provided by a simple inverting operational amplifier circuit with a gain of $R_{S2}/R_{S1} = 200k/100k = 2$. Horowitz and Hill provide a table in [12] that compares the noise response of a wide range of operational

amplifiers. The ultralow noise high speed LT1028 precision opamp was selected due to its availability, low voltage noise characteristics and inclusion in the LTspice component library.

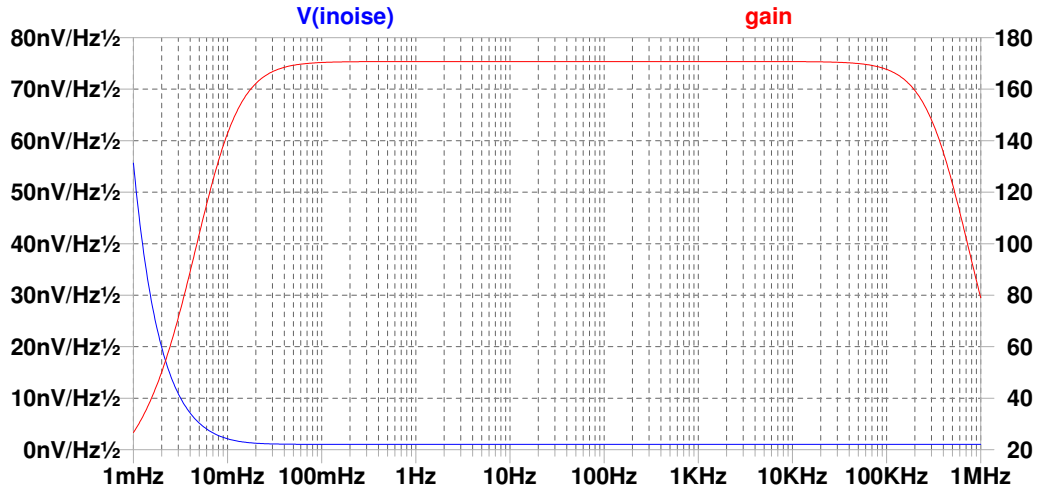


Figure 4.8: Simulation results for the DSS20201L at $I_C = 1$ mA including the effect of the transistor's flicker noise.

Figure 4.9 shows the equivalent input noise and gain of the circuit using the DSS20201L BJT at $I_C = 1$ mA with a secondary amplification stage using the LT1028 opamp. This simulation also included the effect of the transistors flicker noise. The noise at 1 mA was found to be almost 2000 times larger than that measured with the assumptions that the noise added by the operational amplifier would be negligible and that the transistor flicker noise was accounted for.

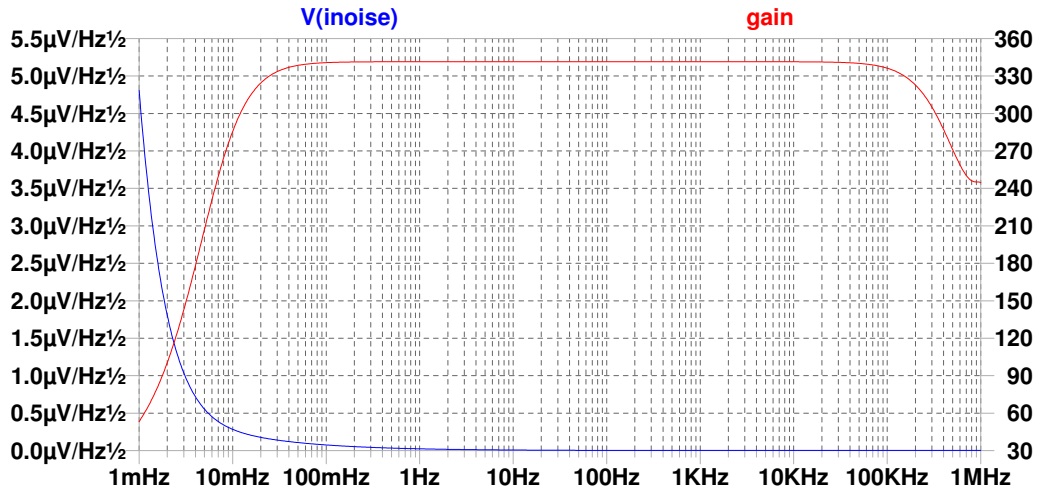


Figure 4.9: Simulation results for DSS20201L at $I_C = 1$ mA including the effect of the transistor's flicker noise and noise of a secondary amplification stage.

Settling Time

Because so much focus was placed on achieving the desired low noise response, the effect of the chosen capacitor values on the transient response wasn't intially considered. By default, LTspice simulates the transient response at the operating point without considering the time taken for the circuit to settle at that point. As a result, it was only when the circuits were built and tested that the issues with the transient response were observed.

The large capacitors required for achieving low noise at the sub 1 Hz frequency range take a very long time to charge. As a result, the circuit takes an extremely long time to settle at the operating point. The output of the circuit was measured with an oscilloscope for the case where no input signal is applied. The time taken until the circuit reached its steady state value was measured and found to be over 15 minutes.

Conclusion

These design flaws make the common emitter input stage completely unsuitable for the desired FLL system due to the requirement for low noise at very low frequencies and the need for the circuit to quickly respond to voltage inputs. The use of coupling and bypass capacitors in the circuit is not an option due to the issues with charging times. As a result, an input stage with DC coupling is required.

4.3 Differential Amplifier

This design uses a differential amplifier with current source for the input stage. Differential amplifiers are DC coupled so the issues caused by capacitors in the common emitter amplifier design are avoided. Two different differential amplifier options were considered. The first option uses a single differential amplifier with current source and high gain. The second option uses two cascaded differential amplifier stages each with their own current source. The gain of the individual stages is smaller than that of the single stage design, but the combined gain is significantly larger. Both designs are followed by an instrumentation amplifier to convert the differential output to a single-ended output.

At the time the differential amplifiers were designed, more information about the M2700 SQUID was available. This included the value of the SQUID resistance at the output pins without a transformer (5 Ω) and with a transformer (125 Ω). This allowed for more accurate simulations since the source resistance of the amplifier was known and not assumed as it was in Section 4.2.

The table of low noise matched BJT pairs in [12] was used to select appropriate transistors for the design. The list was narrowed down to the options with detailed information available, the best noise characteristics and availability from electronics suppliers. From these, the option with the best matching characteristics was chosen: the SSM2212 npn matched pair from Analog Devices [44]. This matched pair also has a high β value of between 500 and 600. For all calculations using assumptions in this section, β was assumed to be 500. In addition, $V_{BE(on)} = 0.7\ V$ throughout this section.

The Spice model for the SSM2212 matched pair BJTs was obtained from the manufacturer's website. As with the transistors for the common emitter amplifier, this model did not include a flicker noise exponent parameter KF. The datasheet for these transistors included a plot of the noise voltage density at different current levels, so the corner frequency f_L can be obtained from the plot as needed to accurately model the flicker noise in LTspice.

The differential amplifiers and current sources use the +5 V and -5 V regulated voltage supplies, while the instrumentation amplifier uses the +12 V and -12 V supplies (see Section 3.2). R_{B1} and R_{B2} are used to represent the source resistance seen by the differential amplifiers (5 Ω or 125 Ω depending whether the optional transformer is used).

Figure 4.10 on the next page shows the basic circuit configuration for a differential amplifier.

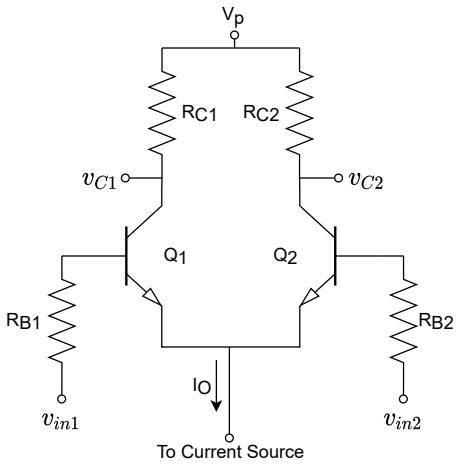


Figure 4.10: Basic circuit diagram of a differential amplifier.

4.3.1 Current Source

A simple two transistor current mirror was chosen to provide the desired I_C values for the differential amplifiers. A two transistor configuration was preferred over other options due to the low number of components required. Circuits with more components contain more sources of noise. Figure 4.11 shows the circuit diagram of the proposed current source.

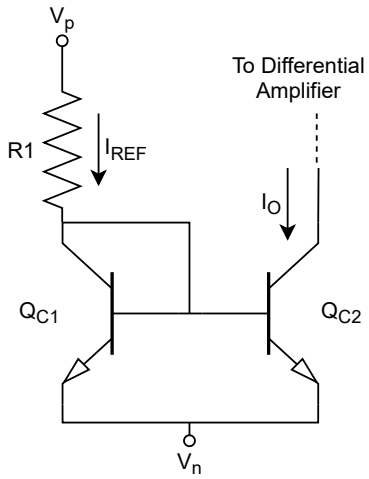


Figure 4.11: Two transistor current source.

Basic Circuit Analysis:

The formulae to calculate the currents in the circuit are

$$I_{REF} = \frac{V_p - V_{BE(on)} - V_n}{R_1} \tag{4.31}$$

$$I_O = \frac{I_{REF}}{1 + \frac{2}{\beta_{C1}}} \tag{4.32}$$

Since β is very large ($\beta_{C1} = \beta_{C2} \approx 500$) it can be assumed that

$$I_O \approx I_{REF} \tag{4.33}$$

After analysing the plot of noise voltage density against frequency in the SSM2212 datasheet [44], it was decided to design for three different collector currents through the differential amplifier BJTs. This would allow for a comparison of the noise results at these currents. The chosen currents are $I_C = 500\ \mu$A, 1 mA and 2 mA. The current source in Figure 4.11 needs to be able to supply twice the desired collector current of the differential amplifier BJTs. This means that the current source needs to be designed for $I_o = I_{REF} = 1$ mA, 2 mA and 4 mA. The values of R_1 required to produce these currents are calculated as 9.3 kΩ, 4.65 kΩ and 2.325 kΩ respectively.

Noise Analysis:

Figure 4.12 shows the small signal equivalent circuit of the two transistor current source including all thermal, shot and flicker noise sources. R_d in this figure is the input resistance of the differential amplifier as seen by the current source. The calculation of this resistance is shown in Sections 4.3.3 and 4.3.4. Since R_d is just a representation of the resistance of the differential amplifier, it has no thermal noise contribution.

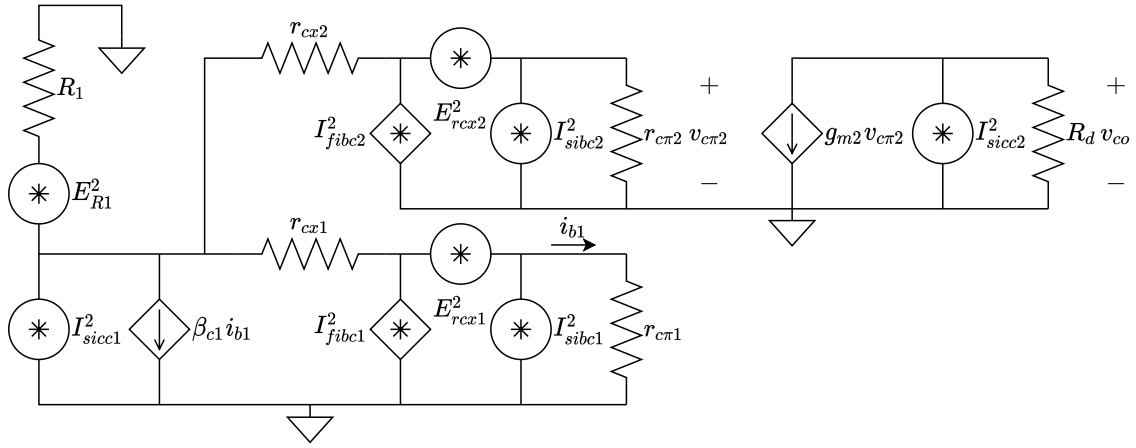


Figure 4.12: Small signal equivalent circuit of the current source including noise sources.

The small signal circuit parameters are calculated as

$$r_{c\pi1} = r_{c\pi2} = \frac{\beta_C V_T}{I_{REF}} \tag{4.34}$$

$$r_{co1} = r_{co2} = \frac{V_A}{I_{REF}} \tag{4.35}$$

$$g_{mc1} = g_{mc2} = \frac{I_{REF}}{V_T} \tag{4.36}$$

For the value of V_A from the Spice model (150), the output resistances r_{co1} and r_{co2} for all three of the current values are very large when compared with R_d and the other resistances in the circuit. As a result, they are ignored in the noise calculations.

The equivalent noise of the current source at it's output (v_{CO}) needs to be calculated so that it can easily be referred to the outputs of the differential amplifiers in Sections 4.3.3 and 4.3.4. An important equation needed to determine this is the gain

$$A_{CC} = \frac{v_{CO}}{v_{c\pi2}} = g_{cm2} Rd \tag{4.37}$$

Equations (4.38)-(4.46) calculate the base value of each noise source in the circuit.

$$E_{R1}^2 = 4kTR_1 \tag{4.38}$$

$$E_{rcx1}^2 = 4kTr_{cx1} \tag{4.39}$$

$$E_{rcx2}^2 = 4kTr_{cx2} \tag{4.40}$$

$$I_{sicc1}^2 = 2qI_{Cc1} \tag{4.41}$$

$$I_{sicc2}^2 = 2qI_{Cc2} \tag{4.42}$$

$$I_{sibc1}^2 = 2qI_{Bc1} \tag{4.43}$$

$$I_{sibc2}^2 = 2qI_{Bc2} \tag{4.44}$$

$$I_{fibc1}^2 = \frac{2qf_L I_{Bc1}^{\gamma}}{f} \tag{4.45}$$

$$I_{fibc2}^2 = \frac{2qf_L I_{Bc2}^{\gamma}}{f} \tag{4.46}$$

The plot of noise voltage density against frequency in the SSM2212 datasheet is used to determine an appropriate value for f_L in the flicker noise equations. The plot contains three different noise curves at 1 μA, 10 μA and 1 mA. Since the required collector currents are close to 1 mA, an estimate of the corner frequency is made from the corresponding curve. The corner frequency is estimated at $f_L = 1$ Hz. This value is used in all transistor flicker noise equations in this chapter.

The equivalent noise seen at v_{CO} can be calculated for each noise source. The equations obtaining E_{ocN}^2 for each noise source are detailed below where N is replaced by the subscript of the relevant noise source.

Thermal noise contributions at v_{CO}:

$$E_{ocR1}^2 = E_{R1}^2 \times \left(\frac{r_{c\pi 2}}{r_{c\pi 2}+r_{cx2}}\right)^2 \times \left(\frac{(r_{c\pi 2}+r_{cx2})||(\frac{r_{c\pi 1}+r_{cx1}}{\beta_{C1}+1})}{(r_{c\pi 2}+r_{cx2})||(\frac{r_{c\pi 1}+r_{cx1}}{\beta_{C1}+1})+R_1}\right)^2 \times A_{CC}^2 \tag{4.47}$$

$$E_{ocrcx1}^2 = E_{rcx1}^2 \times \left(\frac{r_{c\pi 2}}{r_{c\pi 2}+r_{cx2}}\right)^2 \times \left(\frac{(\beta_{C1}+1)(R_1||(r_{c\pi 2}+r_{cx2}))}{r_{c\pi 1}+r_{cx1}+(\beta_{C1}+1)(R_1||(r_{c\pi 2}+r_{cx2}))}\right)^2 \times A_{CC}^2 \tag{4.48}$$

$$E_{ocrcx2}^2 = E_{rcx2}^2 \times \left(\frac{r_{c\pi 2}}{r_{c\pi 2}+r_{cx2}+R_1||(\frac{r_{c\pi 1}+r_{cx1}}{\beta_{C1}+1})}\right)^2 \times A_{CC}^2 \tag{4.49}$$

Shot noise contributions at v_{CO}:

$$E_{ocsicc1}^2 = I_{sicc1}^2 \times \left(\frac{r_{c\pi 2}}{r_{c\pi 2}+r_{cx2}}\right)^2 \times (R_1||(r_{c\pi 2}+r_{cx2})||(\frac{r_{c\pi 1}+r_{cx1}}{\beta_{C1}+1}))^2 \times A_{CC}^2 \tag{4.50}$$

$$E_{ocsicc2}^2 = I_{sicc2}^2 \times (R_d)^2 \tag{4.51}$$

$$E_{ocsibc1}^2 = I_{sibc1}^2 \times \left(\frac{r_{c\pi 2}}{r_{c\pi 2}+r_{cx2}}\right)^2 \times \left(\frac{1}{\frac{1}{r_{c\pi 1}}+\frac{1}{r_{cx1}}(1-\frac{\frac{1}{r_{cx1}}-\frac{\beta_{C1}}{r_{c\pi 1}}}{\frac{1}{R_1}+\frac{1}{r_{cx1}}+\frac{1}{r_{c\pi 2}+r_{cx2}}})}\right)^2 \times \left(\frac{\frac{1}{r_{cx1}}-\frac{\beta_{C1}}{r_{c\pi 1}}}{\frac{1}{R_1}+\frac{1}{r_{cx1}}+\frac{1}{r_{c\pi 2}+r_{cx2}}}\right)^2 \times A_{CC}^2 \tag{4.52}$$

$$E^2_{ocsibc2} = I^2_{sibc2} \times (r_{c\pi 2}||(r_{cx2} + R_1||(\frac{r_{c\pi 1} + r_{cx1}}{\beta_{C1} + 1})))^2 \times A^2_{CC} \tag{4.53}$$

Flicker noise contributions at v_{CO}:

$$\begin{aligned} E^2_{ocfibc1} = I^2_{fibc1} \times (\frac{r_{c\pi 2}}{r_{c\pi 2} + r_{cx2}})^2 \times (\frac{1}{\frac{1}{r_{c\pi 1}} + \frac{1}{r_{cx1}}(1 - \frac{\frac{1}{r_{cx1}} - \frac{\beta_{C1}}{r_{c\pi 1}}}{\frac{1}{R_1} + \frac{1}{r_{cx1}} + \frac{1}{r_{c\pi 2} + r_{cx2}}})})^2 \\ \times (\frac{\frac{1}{r_{cx1}} - \frac{\beta_{C1}}{r_{c\pi 1}}}{\frac{1}{R_1} + \frac{1}{r_{cx1}} + \frac{1}{r_{c\pi 2} + r_{cx2}}})^2 \times A^2_{CC} \end{aligned} \tag{4.54}$$

$$E^2_{ocfibc2} = I^2_{fibc2} \times (r_{c\pi 2}||(r_{cx2} + R_1||(\frac{r_{c\pi 1} + r_{cx1}}{\beta_{C1} + 1})))^2 \times A^2_{CC} \tag{4.55}$$

4.3.2 Instrumentation Amplifier

An instrumentation amplifier is used to convert the differential output of the differential amplifier stages to a single-ended output. This circuit configuration has a high input impedance and provides easy gain control [43]. It is typically implemented using three operational amplifiers and seven resistors. Alternatively an instrumentation amplifier IC could be used. For this research the instrumentation amplifier is implemented using discrete components. The LT1028 operational amplifier discussed in Section 4.2.5 was chosen for the design. Figure 4.13 shows the circuit configuration of the proposed instrumentation amplifier.

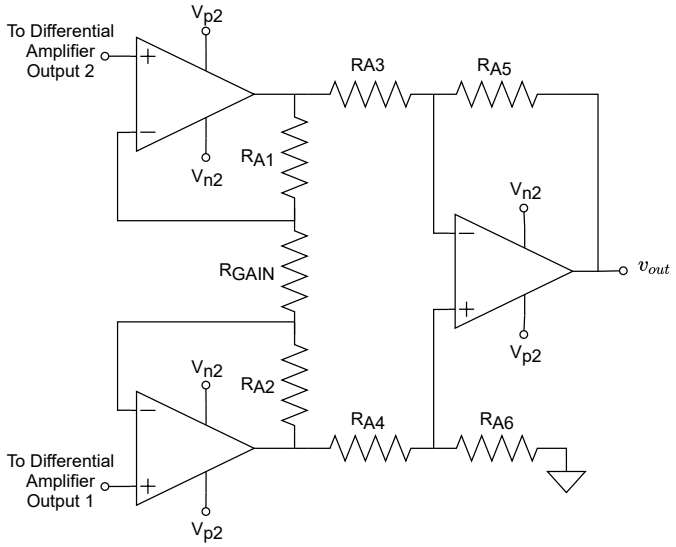


Figure 4.13: Circuit configuration of an instrumentation amplifier.

For typical operation of an instrumentation amplifier, resistor values are chosen such that $R_{A1} = R_{A2} = R_A$, $R_{A3} = R_{A4} = R_B$ and $R_{A5} = R_{A6} = R_C$. According to [43], the formula for the gain is then

$$A_{vi} = \frac{R_C}{R_B}(1 + \frac{2R_A}{R_{GAIN}}) \tag{4.56}$$

Since the circuit is designed with the focus on converting the differential amplifier output to a single-ended output, it is not used as a large gain stage. The majority of the system gain is provided by the differential amplifier stages and secondary amplification stage discussed in

Section 4.6. As a result, it is assumed that $R_A = R_B = R_C$ and $R_{GAIN} = 2R_A$. The gain of the instrumentation amplifier is then $A_{vi} = 2$.

Noise Analysis:

Figure 4.14 shows the instrumentation amplifier circuit including all noise sources. R_{od1} and R_{od2} are the output resistances seen by the instrumentation amplifier inputs at the preceding differential amplifier stage's outputs.

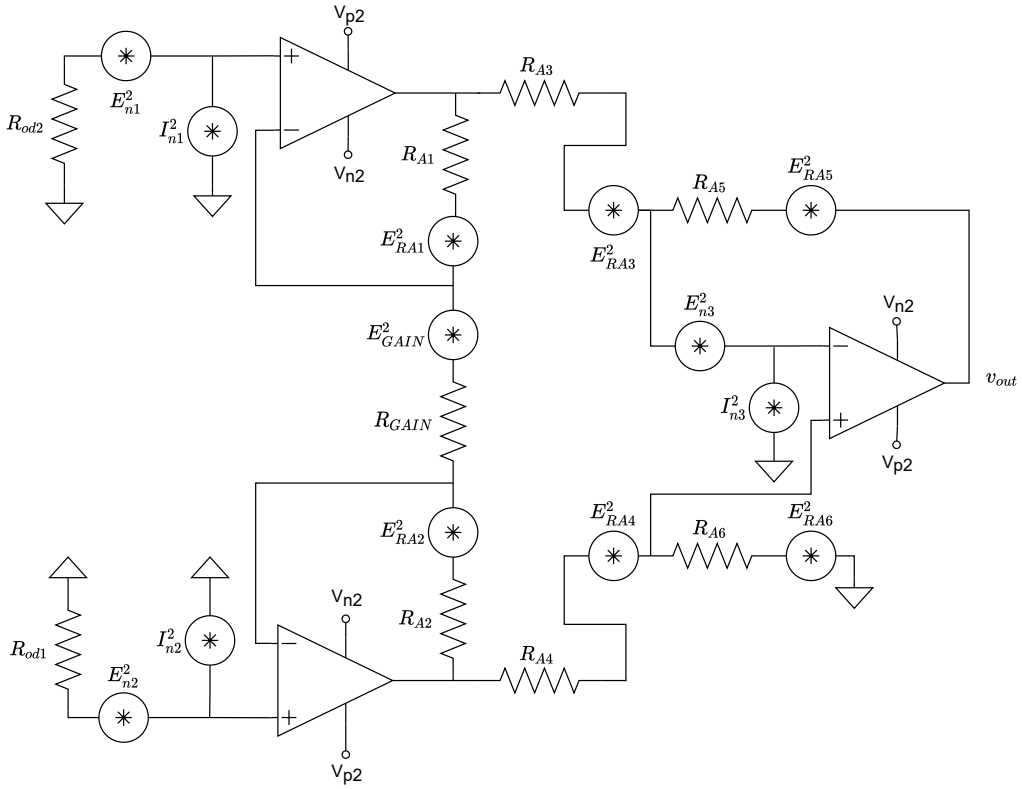


Figure 4.14: Diagram of an instrumentation amplifier including all noise sources.

Equations (4.57) and (4.58) calculate the base value of the thermal noise sources in the circuit.

$$E^2_{RA} = 4kTR_A \tag{4.57}$$

$$E^2_{RGAIN} = 4kTR_{GAIN} \tag{4.58}$$

The voltage and current noise of the LT1028 operational amplifier is obtained from graphs in the datasheet. These noise values need to be further subdivided into flatband and flicker noise. Since the formula for $1/f$ noise is generally taken as $E^2_f = \frac{K}{f}$ where K is a constant, we can determine the formula for the flicker noise response for both voltage and current noise. Taking one point from the $1/f$ region of the plot of noise density against frequency and rearranging the formula gives $K = E^2_f f$. Since we now have the constant K, we should be able to determine the flicker noise for any frequency.

This method of determining the flicker noise response is not entirely accurate since it assumes perfect $1/f$ characteristics, but simulation shows that it produces a response that is close enough to the expected flicker noise. If the worst case noise is assumed we have

$$E_{n1} = E_{n2} = E_{n3} = 1.2\,nV/\sqrt{\text{Hz}}$$
$$I_{n1} = I_{n2} = I_{n3} = 1.8\,pA/\sqrt{\text{Hz}}$$
$$E_{nf1} = E_{nf2} = E_{nf3} = \frac{10\,nV/\sqrt{\text{Hz}} \times \sqrt{0.1}}{\sqrt{f}}$$
$$I_{nf1} = I_{nf2} = I_{nf3} = \frac{12\,pA/\sqrt{\text{Hz}} \times \sqrt{10}}{\sqrt{f}}$$

The equivalent noise at the output of the instrumentation amplifier is then

$$E_{oIA}^2 = 6 \times E_{RA}^2 + E_{RGAIN}^2 + (2)^2(E_{n1}^2 + E_{nf1}^2 + E_{n2} + E_{nf2}^2 + (I_{n2}^2 + I_{nf2}^2)R_{od1}^2 + (I_{n1}^2 + I_{nf1}^2)R_{od2}^2) + (2)^2(E_{n3}^2 + E_{nf3}^2 + (I_{n3}^2 + I_{nf3}^2)(\frac{R_A}{2})^2) \tag{4.59}$$

4.3.3 Single Stage Differential Amplifier

Figure 4.15 shows the circuit diagram for a single stage differential amplifier with current source and instrumentation amplifier. The differential inputs v_{in1} and v_{in2} would be connected to the voltage output of the SQUID after the optional transformer. The source resistance seen by the differential amplifier inputs is then $R_{B1} = R_{B2} = 125\ \Omega$. Since the input resistance of an instrumentation amplifier is so high we assume that it has no detrimental impact on the differential gain of the circuit.

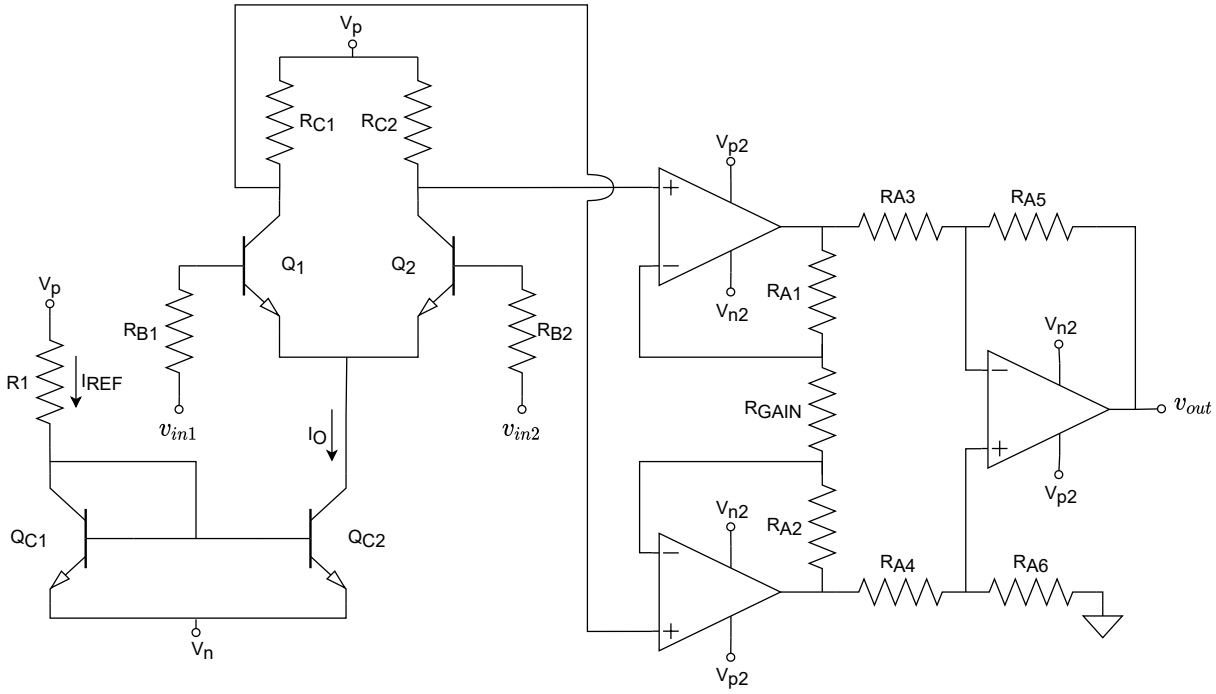


Figure 4.15: Single stage differential amplifier with current source and instrumentation amplifier output stage.

Basic Circuit Analysis:

The small signal parameters for the differential amplifier are

$$r_{\pi 1} = \frac{\beta_1 V_T}{I_{C1}} \qquad \text{and} \qquad r_{\pi 2} = \frac{\beta_2 V_T}{I_{C2}} \tag{4.60}$$

$$r_{o1} = \frac{V_A}{I_{C1}} \qquad \text{and} \qquad r_{o2} = \frac{V_A}{I_{C2}} \tag{4.61}$$

$$g_{m1} = \frac{I_{C1}}{V_T} \qquad \text{and} \qquad g_{m2} = \frac{I_{C2}}{V_T} \tag{4.62}$$

For the design process we assume that the transistors are perfectly matched and that

$$\begin{gathered} I_{C1} = I_{C2} = I_C \\ \beta_1 = \beta_2 = \beta \\ r_{\pi 1} = r_{\pi 2} = r_\pi \\ r_{x1} = r_{x2} = r_x \\ r_{o1} = r_{o2} = r_o \\ R_{C1} = R_{C2} = R_C \end{gathered}$$

There are two important gain figures for a differential amplifier. The differential gain is the gain that amplifies a differential input signal to a differential output. The common-mode gain is the gain that amplifies a common-mode input signal to a differential output. Common-mode gain is undesirable in a circuit and the aim is to keep it as low as possible. The two gains are

$$A_d = \frac{-\beta Rc||r_o}{r_\pi + r_x + R_B} \tag{4.63}$$

$$A_c = 0 \tag{4.64}$$

This means that a perfectly matched differential amplifier has zero common-mode gain.

Since this design only uses a single differential amplifier stage, we want the gain of this stage to be very large. One concern is that the offset voltage of the SQUID is also amplified and that amplifying this signal too much will cause the signal to clip as it approaches the voltage rails. Therefore the differential amplifier needs to have a large voltage swing range with the DC offset at the two outputs very close to 0 V. As mentioned in Section 4.3.1, the circuit is designed for $I_C = 500$ μA, 1 mA and 2 mA. For these values we can determine the resistance R_C that would produce a DC offset of 0 V at the collector of each transistor.

$$R_C = \frac{V_p}{I_C} \tag{4.65}$$

The gain corresponding to the resistance value can then be calculated. This gain is found to be close to -190 for each of the three I_C values under consideration. The circuit is then designed for a slightly smaller gain to ensure that the transistor operates in the active region. The gain is chosen as A_d = -180. The R_C values that would theoretically produce this gain for $I_C = 500$ μA, 1 mA and 2 mA are $R_C = 9.41$ kΩ, 4.73 kΩ and 2.39 kΩ respectively.

The differential amplifier is then simulated and the resistances are adjusted to achieve a gain magnitude just larger than 180 for each I_C value. The resistances at which this gain was obtained were $R_C = 9.46$ kΩ, 4.81 kΩ and 2.48 kΩ. These values are extremely close to the theoretically calculated values.

With the differential gain equal to A_d = -180 and the gain of the instrumentation amplifier equal to $A_{vi} = 2$, the combined gain of the two stages is -360. The maximum offset voltage of the M2700 SQUID is expected to be in the region of 510 μV and under. Taking an offset voltage larger than this value to test the limits of the design is necessary since the voltage offset might

exceed the expected value. An offset with an amplitude of 1 mV is assumed. This translates to 5 mV after the transformer at the differential amplifier's input. For a gain of 360, the output of the instrumentation amplifier due to the SQUID offset voltage should be a maximum of 1.8 V. This is well below the voltage rails and the signal can therefore be safely amplified without clipping.

Noise Analysis:

Figure 4.16 shows the small signal equivalent circuit of the differential amplifier including all noise sources. E_{CO}^2 is the equivalent noise of the current source at its output as calculated in Section 4.3.1. The instrumentation amplifier is not shown in the diagram, but the noise contributions are as calculated in Section 4.3.2 and the gain is $A_{vi} = 2$.

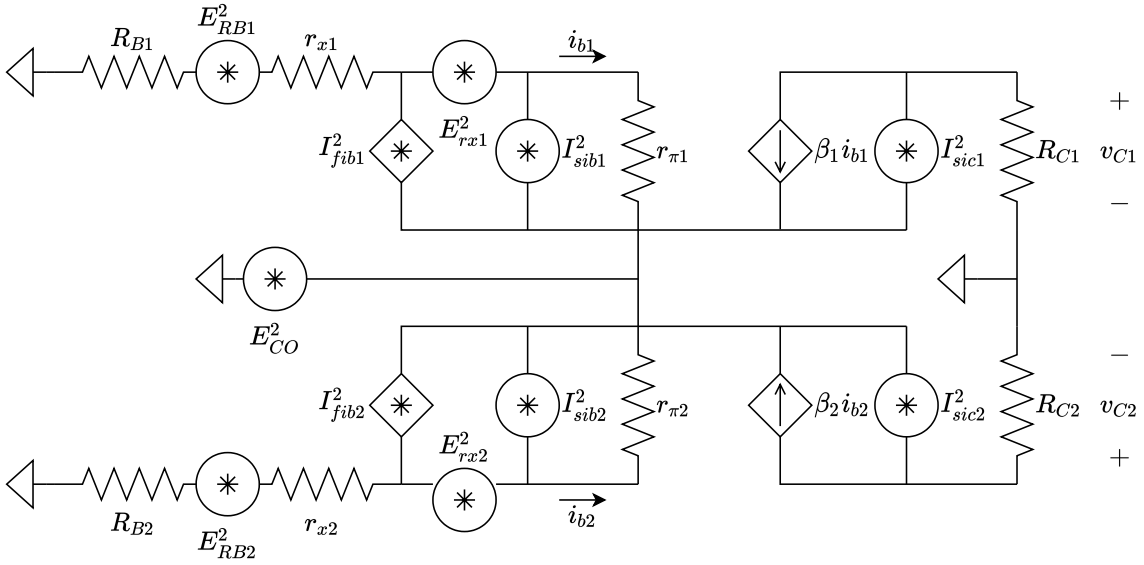


Figure 4.16: Small signal equivalent circuit of the single stage differential amplifier including all noise sources. E_{CO}^2 is the equivalent noise of the current source at its output as calculated in Section 4.3.1.

A number of important values are required to accurately calculate the total output noise of the system including all noise contributions from the current source, differential amplifier and instrumentation amplifier.

The current source noise equations from Section 4.3.1 require the input resistance of the differential amplifier as seen by the current source. This value is calculated as

$$R_d = \frac{r_{\pi 1} + r_{x1} + R_{B1}}{\beta_1 + 1} || \frac{r_{\pi 2} + r_{x2} + R_{B2}}{\beta_2 + 1} \tag{4.66}$$

The instrumentation amplifier noise equations from Section 4.3.2 require the output resistance of the differential amplifier at each differential output. The resistance at the collector of Q_1 is $R_{od1} \approx R_{C1}$. Likewise, the resistance at the collector of Q_2 is $R_{od2} \approx R_{C2}$.

The differential gain of the circuit without the assumptions used to design the differential amplifier is

$$A_d = -\left(\frac{\beta_1 R_{C1} || r_{o1}}{2(r_{\pi 1} + r_{x1} + R_{B1})} + \frac{\beta_2 R_{C2} || r_{o2}}{2(r_{\pi 2} + r_{x2} + R_{B2})}\right) \tag{4.67}$$

Another important circuit gain is from the output of the current source to the output of the differential amplifier. This gain determines the noise contribution of the current source noise E_{CO}^2 at the output of the differential amplifier. The current source noise is essentially a common-mode signal, so it is necessary to determine the differential mode output produced from this signal. The equation for this gain is

$$A_{cd} = \frac{\beta_2 R_{C2}||r_{o1}}{r_{\pi 2} + r_{x2} + R_{B2}} - \frac{\beta_1 R_{C1}||r_{o2}}{r_{\pi 1} + r_{x1} + R_{B1}} \tag{4.68}$$

In a perfectly matched system this gain is equal to zero and the current source contributes no noise at the output of the differential amplifier. Any mismatch in R_C, I_C or β values gives a non-zero gain. The resistors chosen for R_C are thus chosen with the best possible tolerance values to ensure they match as closely as possible. Precision metal foil resistors with a tolerance of 0.01% are ideally suited for this application since they are both low noise and low tolerance [14].

Equations (4.69)-(4.80) calculate the base value of each noise source in Figure 4.16.

$$E_{RB1}^2 = 4kTR_{B1} \tag{4.69}$$

$$E_{RB2}^2 = 4kTR_{B2} \tag{4.70}$$

$$E_{RC1}^2 = 4kTR_{C1} \tag{4.71}$$

$$E_{RC2}^2 = 4kTR_{C2} \tag{4.72}$$

$$E_{rx1}^2 = 4kTr_{x1} \tag{4.73}$$

$$E_{rx2}^2 = 4kTr_{x2} \tag{4.74}$$

$$I_{sic1}^2 = 2qI_{C1} \tag{4.75}$$

$$I_{sic2}^2 = 2qI_{C2} \tag{4.76}$$

$$I_{sib1}^2 = 2qI_{B1} \tag{4.77}$$

$$I_{sib2}^2 = 2qI_{B2} \tag{4.78}$$

$$I_{fib1}^2 = \frac{2qf_L I_{B1}^{\gamma}}{f} \tag{4.79}$$

$$I_{fib2}^2 = \frac{2qf_L I_{B2}^{\gamma}}{f} \tag{4.80}$$

The noise contributions of the current source at its output are obtained from Section 4.3.1. The equations for the noise contributions of the instrumentation amplifier at its output are given in Section 4.3.2. Since the output of the instrumentation amplifier is the output of the full LNA design, these equations do not undergo any additional adjustments. The noise contributions of the differential amplifier noise sources at the output of the instrumentation amplifier (v_{out}) are given below.

Thermal noise contributions of the differential amplifier at v_{out}:

$$E_{oRB1}^2 = E_{RB1}^2 \times (\frac{2r_{\pi 1} + r_{x1}}{2r_{\pi 1} + r_{x1} + R_{B1}})^2 \times A_d^2 \times A_{vi}^2 \tag{4.81}$$

$$E_{oRB2}^2 = E_{RB2}^2 \times (\frac{2r_{\pi 2} + r_{x2}}{2r_{\pi 2} + r_{x2} + R_{B2}})^2 \times A_d^2 \times A_{vi}^2 \tag{4.82}$$

$$E_{oRC1}^2 = E_{RC1}^2 \times A_{vi}^2 \tag{4.83}$$

$$E_{oRC2}^2 = E_{RC2}^2 \times A_{vi}^2 \tag{4.84}$$

$$E_{orx1}^2 = E_{rx1}^2 \times (\frac{2r_{\pi 1}}{2r_{\pi 1} + r_{x1} + R_{B1}})^2 \times A_d^2 \times A_{vi}^2 \tag{4.85}$$

$$E_{orx2}^2 = E_{rx2}^2 \times (\frac{2r_{\pi 2}}{2r_{\pi 2} + r_{x2} + R_{B2}})^2 \times A_d^2 \times A_{vi}^2 \tag{4.86}$$

Shot noise contributions of the differential amplifier at v_{out}:

$$E_{osic1}^2 = I_{sic1}^2 \times (R_{C1}||ro1)^2 \times A_{vi}^2 \tag{4.87}$$

$$E_{osic2}^2 = I_{sic2}^2 \times (R_{C2}||ro2)^2 \times A_{vi}^2 \tag{4.88}$$

$$E_{osib1}^2 = I_{sib1}^2 \times ((R_{B1} + r_{x1})||(2r_{\pi 1}))^2 \times A_d^2 \times A_{vi}^2 \tag{4.89}$$

$$E_{osib2}^2 = I_{sib2}^2 \times ((R_{B2} + r_{x2})||(2r_{\pi 2}))^2 \times A_d^2 \times A_{vi}^2 \tag{4.90}$$

Flicker noise contributions of the differential amplifier at v_{out}:

$$E_{ofib1}^2 = I_{fib1}^2 \times ((R_{B1} + r_{x1})||(2r_{\pi 1}))^2 \times A_d^2 \times A_{vi}^2 \tag{4.91}$$

$$E_{ofib2}^2 = I_{fib2}^2 \times ((R_{B2} + r_{x2})||(2r_{\pi 2}))^2 \times A_d^2 \times A_{vi}^2 \tag{4.92}$$

Noise contribution of the current source at v_{out}:

$$E_{oco}^2 = E_{co}^2 \times A_{cd}^2 \times A_{vi}^2 \tag{4.93}$$

Simulation Results:

The hand calculations were performed with the assumption that $\beta_1 = \beta_2 = \beta_{C1} = \beta_{C2} = 500$ and $I_{Cc1} = I_{Cc2} = 2I_{C1} = 2I_{C2}$. In addition, it was assumed that resistors with a tolerance of 0.01% were used. To account for the effect of mismatched resistors on circuit noise, both the hand calculations and simulation used $R_{C2} = R_{C1} \times 1.0001$.

The equivalent input noise for the different I_C designs was calculated by dividing the total equivalent output noise by the full gain ($A_d \times A_{vi}$). The results obtained from hand calculations were then plotted using MATLAB so that they could be directly compared with the equivalent input noise graphs obtained from simulation.

Tables D.1, D.2 and D.3 in Appendix D contain a comparison of the hand calculated and simulated output noise contributions of every noise source in the circuit when I_C of the differential amplifier is chosen as 500 μA, 1mA and 2 mA respectively.

Figures 4.17, 4.19 and 4.21 show the plots of equivalent input noise and the magnitude of the gain obtained from simulation for $I_C = 500$ μA, 1 mA and 2 mA respectively. Figures 4.18, 4.20 and 4.22 show the plot of equivalent input noise obtained via calculation for $I_C = 500$ μA, 1 mA and 2 mA respectively.

Table 4.4 contains a summary of the calculated and simulated equivalent input noise results obtained for each of the three I_C values. From the results in the table and the plots of equivalent input noise it is confirmed that the hand calculations correspond extremely well with the simulated results despite the assumptions used.

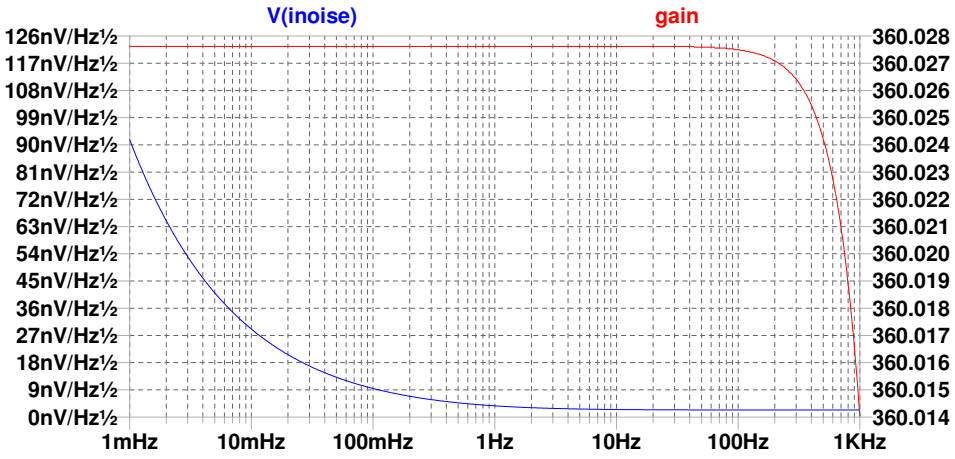


Figure 4.17: Simulation results showing the gain and equivalent input noise when I_C is chosen as 500 μA for a single stage differential amplifier design.

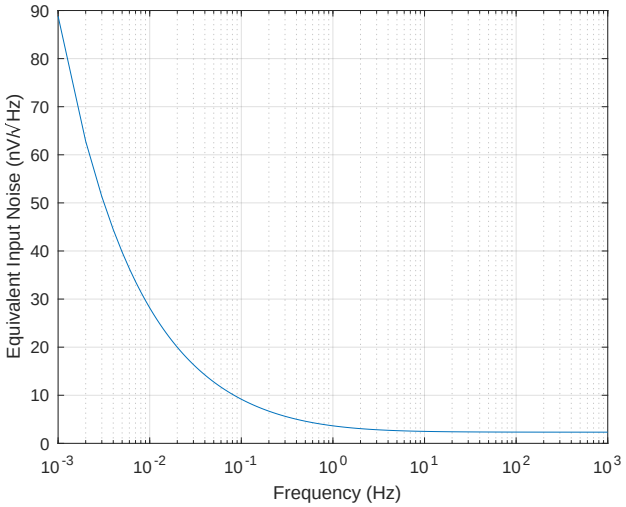


Figure 4.18: Hand calculation results showing the equivalent input noise when I_C is chosen as 500 μA for a single stage differential amplifier design.

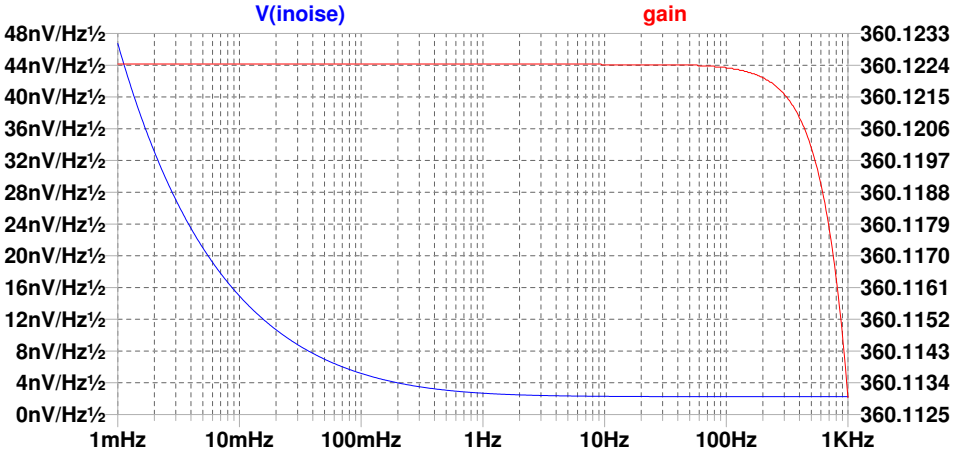


Figure 4.19: Simulation results showing the gain and equivalent input noise when I_C is chosen as 1 mA for a single stage differential amplifier design.

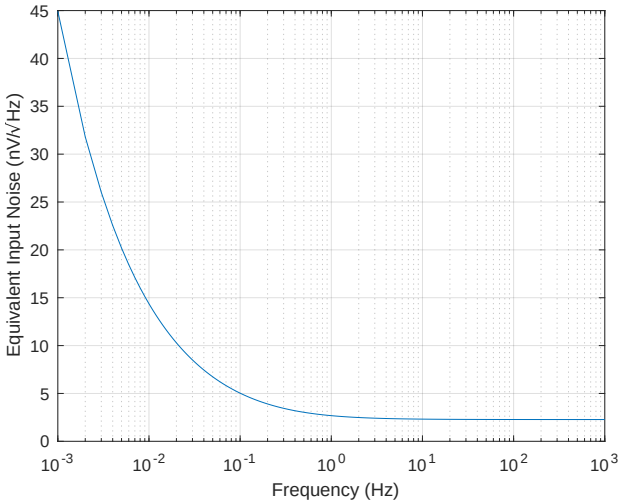


Figure 4.20: Hand calculation results showing the equivalent input noise when I_C is chosen as 1 mA for a single stage differential amplifier design.

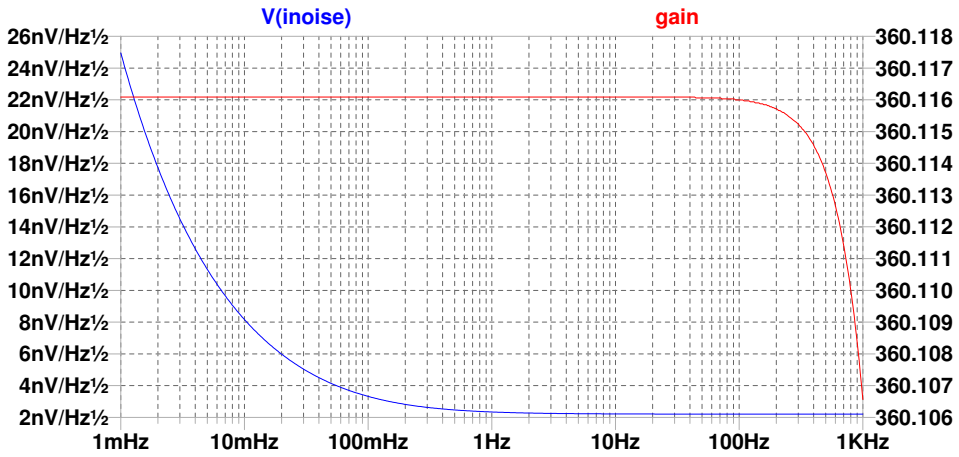


Figure 4.21: Simulation results showing the gain and equivalent input noise when I_C is chosen as 2 mA for a single stage differential amplifier design.

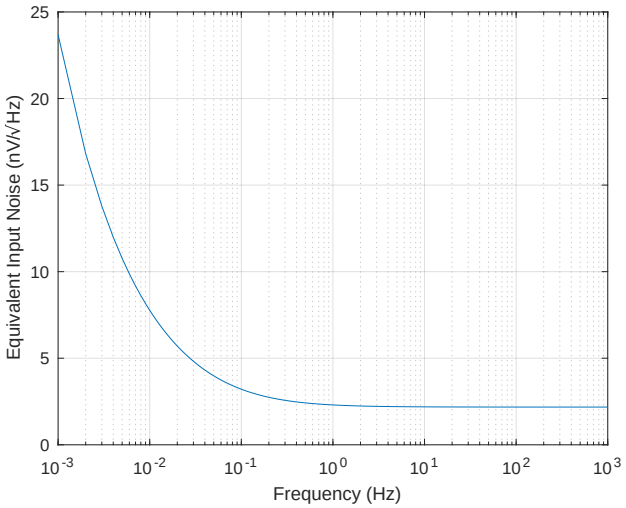


Figure 4.22: Hand calculation results showing the equivalent input noise when I_C is chosen as 2 mA for a single stage differential amplifier design.

It is important to note that all of the results include the effect of thermal noise in resistors R_{B1} and R_{B2}. Since these resistors are a representation of the resistance of the SQUID after the transformer, they do not contribute thermal noise to the equivalent input noise of the amplifier. This means that the equivalent input noise of each amplifier in the flatband is lower than the plots indicate. Since the resistors contribute the same thermal noise for each design, a fair comparison of the three designs could be made without removing the noise contribution of R_{B1} and R_{B2}.

Table 4.4: Summary of the noise response of the single stage differential amplifier pre-amplifier for each I_C value

	500 μA		**1 mA**		**2 mA**	
	Calc.	**Sim.**	**Calc.**	**Sim.**	**Cal.**	**Sim.**
Flatband Noise	2.326 nV/$\sqrt{\text{Hz}}$	2.360 nV/$\sqrt{\text{Hz}}$	2.230 nV/$\sqrt{\text{Hz}}$	2.248 nV/$\sqrt{\text{Hz}}$	2.179 nV/$\sqrt{\text{Hz}}$	2.205 nV/$\sqrt{\text{Hz}}$
Noise at 1 mHz	88.815 nV/$\sqrt{\text{Hz}}$	91.742 nV/$\sqrt{\text{Hz}}$	44.925 nV/$\sqrt{\text{Hz}}$	46.730 nV/$\sqrt{\text{Hz}}$	23.680 nV/$\sqrt{\text{Hz}}$	24.953 nV/$\sqrt{\text{Hz}}$

It was initially assumed that the voltage noise of the operational amplifiers would be the largest source of noise from the instrumentation amplifier stage. As such, the LT1028 operational amplifier was chosen due to its low voltage noise. This was an incorrect assumption to make, and the focus should have been on choosing an operational amplifier with low current noise instead. The results from Tables D.1, D.2 and D.3 clearly indicate that the current noise has a much larger noise contribution than the voltage noise. This is due to the large R_C values used in the differential amplifier. In particular, the flicker current noise of the first two operational amplifiers has a highly detrimental effect on the equivalent input noise of the entire circuit. For all three designs, the flicker current noise contribution of the first two operational amplifiers was the highest flicker noise contribution in the entire circuit.

Of the three designs, the circuit that has $I_C = 2$ mA produced the best noise results for both the flatband and flicker noise regions. This is due to this design having the smallest R_C value which resulted in a smaller noise contribution from the operational amplifier current noise. If the flicker noise of the circuit was not dominated by the LT1028 current noise, the 2mA design would have the worst flicker noise response due to it having the highest current.

To determine the equivalent input noise of each design at the SQUID, the results obtained would still need to be divided by 5 (due to the 5:1 turns transformer between the SQUID and LNA stage). This would give very low flatband noise below 0.5 nV/$\sqrt{\text{Hz}}$. Unfortunately, the flicker noise of this circuit design is still too high for the this amplifier to be suitable for use as the pre-amplifier in the FLL.

4.3.4 Multistage Differential Amplifier

Figure 4.23 on the next page shows the circuit diagram for a two stage cascaded differential amplifier with a separate current source supplying each stage. An instrumentation amplifier is connected at the output to convert the differential output to a single-ended output. The differential inputs v_{in1} and v_{in2} would be connected to the voltage output of the SQUID without including the optional transformer. The source resistance seen by the differential amplifier inputs is then $R_{B1} = R_{B2} = 5\ \Omega$. Once again, it is assumed that the input resistance of the

instrumentation amplifier is high enough that it can be ignored when calculating the gain of the preceding stage.

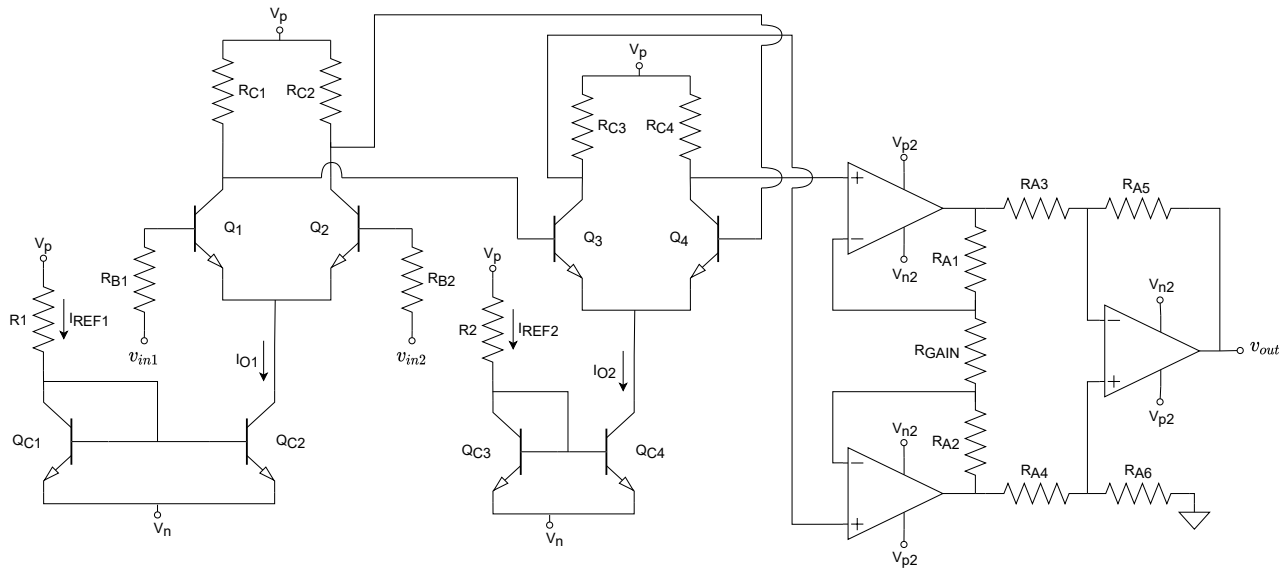


Figure 4.23: Circuit Diagram of a two stage cascaded differential amplifier with separate current sources and an instrumentation amplifier output stage

Basic Circuit Analysis:

The small signal parameters for the differential amplifiers are

$$r_{\pi 1} = \frac{\beta_1 V_T}{I_{C1}} \qquad r_{\pi 2} = \frac{\beta_2 V_T}{I_{C2}} \qquad r_{\pi 3} = \frac{\beta_3 V_T}{I_{C3}} \qquad r_{\pi 4} = \frac{\beta_4 V_T}{I_{C4}} \tag{4.94}$$

$$r_{o1} = \frac{V_A}{I_{C1}} \qquad r_{o2} = \frac{V_A}{I_{C2}} \qquad r_{o3} = \frac{V_A}{I_{C3}} \qquad r_{o4} = \frac{V_A}{I_{C4}} \tag{4.95}$$

$$g_{m1} = \frac{I_{C1}}{V_T} \qquad g_{m2} = \frac{I_{C2}}{V_T} \qquad g_{m3} = \frac{I_{C3}}{V_T} \qquad g_{m4} = \frac{I_{C4}}{V_T} \tag{4.96}$$

For the design process we assume that the transistors are perfectly matched and that the current sources supply the same current to each differential amplifier. The design assumptions are then

$$\begin{gathered} I_{C1} = I_{C2} = I_{C3} = I_{C4} = I_C \\ \beta_1 = \beta_2 = \beta_3 = \beta_4 = \beta \\ r_{\pi 1} = r_{\pi 2} = r_{\pi 3} = r_{\pi 4} = r_\pi \\ r_{x1} = r_{x2} = r_{x3} = r_{x4} = r_x \\ r_{o1} = r_{o2} = r_{o3} = r_{o4} = r_o \\ R_{C1} = R_{C2} = R_{C3} = R_{C4} = R_C \end{gathered}$$

The differential gain of the first differential amplifier is impacted by the loading effect of the second differential amplifier. The input resistance of the second amplifier at each input is $R_{in} \approx 2(r_\pi + r_x)$. Thus the differential gain of the first stage is

$$A_{d1} = \frac{-\beta Rc||R_{in}||r_o}{r_\pi + r_x + R_B} \tag{4.97}$$

The differential gain of the second stage is

$$A_{d2} = \frac{-\beta Rc||r_o}{r_\pi + r_x} \tag{4.98}$$

The common mode gain of each stage for a perfectly matched circuit is

$$A_{c1} = 0 \tag{4.99}$$

$$A_{c2} = 0 \tag{4.100}$$

Since this design uses a two stage differential amplifier, the gain of each stage should be smaller than the gain of the single stage differential amplifier. Since the offset voltage of the SQUID is also amplified, care had to be taken to ensure that the output voltage did not clip for either amplifier. For a single stage differential amplifier, the R_C value was chosen so that the DC offset at the differential outputs would be minimised and the signal wouldn't clip. For the multistage differential amplifier, this is not a suitable design approach since increasing the value of R_C increases the gain of the differential amplifier stage and if the gain of the first stage is too large, then the second stage is likely to clip.

A gain of $A_{d1} = A_{d2} = -40$ was chosen for the two differential amplifiers. For simplification purposes, the loading effect of the second differential amplifier on the first was ignored since it would only reduce the first stage's gain by a small amount. Theoretically, the resistances required to produce this gain at $I_C = 500$ μA, 1 mA and 2 mA are $R_C = 2.801$ kΩ, 1.041 kΩ and 524.4 Ω respectively. The cascaded differential amplifier was then simulated and the resistances adjusted to achieve a total gain ($A_d = A_{d1} \times A_{d2}$) larger than 1600 for each I_C value. The resistances at which this gain was obtained were $R_C = 2.11$ kΩ, 1.07 kΩ and 550 Ω which are very close to the theoretically calculated values.

For this design, it was necessary to check if the offset voltage of the SQUID would cause the output voltage to clip. To do this, the output voltage swing due to the SQUID offset voltage had to be determined for each stage. It was assumed that the gain of each differential stage was -40 and, as before, the amplitude of the SQUID offset voltage was taken as 1 mV. The swing of the first differential amplifier is equal to 1 mV $\times \frac{A_{d1}}{2}$. The swing of the second differential amplifier is 1 mV $\times A_{d1} \times \frac{A_{d2}}{2}$.

Table 4.5 contains the results of calculating the maximum allowable output swing and the output swing due to a SQUID offset of 1 mV. For all three I_C values, the maximum allowable output swing is larger than the swing caused by the SQUID offset voltage. The difference between the maximum swing and expected swing is small, so the SQUID offset voltage can't be much larger than 1 mV, without causing the output signal to clip.

Table 4.5: Calculated maximum allowable output swing and output swing due to SQUID offset for the multistage differential amplifier.

$\mathbf{I_C}$	$\mathbf{R_C}$	**Max swing**	$\mathbf{A_{d1}}$ **swing**	$\mathbf{A_{d2}}$ **swing**
500 μA	2.11 kΩ	1.055 V	20 mV	800 mV
1 mA	1.07 kΩ	1.070 V	20 mV	800 mV
2 mA	550 Ω	1.100 V	20 mV	800 mV

Noise Analysis:

Figure 4.24 shows the small signal equivalent circuit of the two differential amplifier stages including all noise sources. E^2_{CO1} and E^2_{CO2} are the equivalent noise of each of the current sources at their outputs as calculated in Section 4.3.1. The output instrumentation amplifier is not shown in the diagram, but the noise contributions are calculated in Section 4.3.2 and the gain is $A_{vi} = 2$.

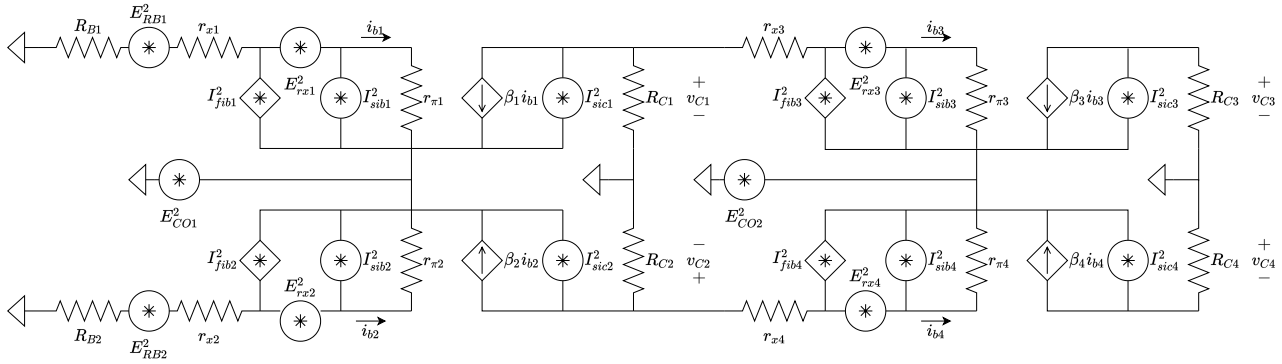


Figure 4.24: Small signal equivalent circuit of the two stage differential amplifier including all noise sources. E^2_{CO1} and E^2_{CO2} are the equivalent noise of the current sources used to supply the first and second differential amplifier respectively.

Once again, a few important values are required to accurately calculate the full output noise of the system including all noise contributions from the current source, differential amplifier and instrumentation amplifier stage.

The current source noise equations from Section 4.3.1 require the input resistance of the differential amplifiers as seen by the current sources. These values are calculated as

$$R_{d1} = \frac{r_{\pi1} + r_{x1} + R_{B1}}{\beta_1 + 1} || \frac{r_{\pi2} + r_{x2} + R_{B2}}{\beta_2 + 1} \tag{4.101}$$

$$R_{d2} = \frac{r_{\pi3} + r_{x3} + R_{C1}}{\beta_3 + 1} || \frac{r_{\pi4} + r_{x4} + R_{C2}}{\beta_4 + 1} \tag{4.102}$$

The instrumentation amplifier noise equations from Section 4.3.2 require the output resistance of the differential amplifier at each differential output. The resistance at the collector of Q_3 is $R_{od1} \approx R_{C3}$. Likewise, the resistance at the collector of Q_4 is $R_{od2} \approx R_{C4}$.

The calculations of the differential gains for each of the differential amplifiers without the assumptions used to design each amplifier are

$$A_{d1} = -\left(\frac{\beta_1 R_{C1} || r_{o1} || R_{in3}}{2(r_{\pi1} + r_{x1} + R_{B1})} + \frac{\beta_2 R_{C2} || r_{o2} || R_{in4}}{2(r_{\pi2} + r_{x2} + R_{B2})}\right) \tag{4.103}$$

$$A_{d2} = -\left(\frac{\beta_3 R_{C3} || r_{o3}}{2(r_{\pi3} + r_{x3})} + \frac{\beta_4 R_{C4} || r_{o4}}{2(r_{\pi4} + r_{x4})}\right) \tag{4.104}$$

Where $R_{in3} \approx 2(r_{\pi3} + r_{x3})$ and $R_{in4} \approx 2(r_{\pi4} + r_{x4})$.

Once again, the gain from the output of each current source to the output of the corresponding differential amplifier is required to determine the noise contribution of E^2_{CO1} and E^2_{CO2} at the

output. The equations for these gains are

$$A_{cd1} = \frac{\beta_2 R_{C2}||R_{in}}{r_{\pi 2} + r_{x2} + R_{B2}} - \frac{\beta_1 R_{C1}||R_{in}}{r_{\pi 1} + r_{x1} + R_{B1}} \tag{4.105}$$

$$A_{cd2} = \frac{\beta_4 R_{C4}||r_{o4}}{r_{\pi 4} + r_{x4} + R_{C2}} - \frac{\beta_3 R_{C3}||r_{o3}}{r_{\pi 3} + r_{x3} + R_{C1}} \tag{4.106}$$

The effect of r_{o1} and r_{o2} is ignored in A_{cd1} for simplification purposes and we take $R_{in} = \frac{R_{in3}+R_{in4}}{2}$. In a perfectly matched system these gains are equal to zero and the current sources contribute no noise at the output of the full amplifier circuit. Any mismatch in R_C, I_C or β values gives a non-zero gain. Once again, the resistors selected for R_C are are chosen as precision metal foil resistors with a tolerance of 0.01% to minimise any mismatch.

Equations (4.107)-(4.128) calculate the base value of each noise source in Figure 4.24.

$$E_{RB1}^2 = 4kTR_{B1} \tag{4.107}$$

$$E_{RB2}^2 = 4kTR_{B2} \tag{4.108}$$

$$E_{RC1}^2 = 4kTR_{C1} \tag{4.109}$$

$$E_{RC2}^2 = 4kTR_{C2} \tag{4.110}$$

$$E_{rx1}^2 = 4kTr_{x1} \tag{4.111}$$

$$E_{rx2}^2 = 4kTr_{x2} \tag{4.112}$$

$$I_{sic1}^2 = 2qI_{C1} \tag{4.113}$$

$$I_{sic2}^2 = 2qI_{C2} \tag{4.114}$$

$$I_{sib1}^2 = 2qI_{B1} \tag{4.115}$$

$$I_{sib2}^2 = 2qI_{B2} \tag{4.116}$$

$$I_{fib1}^2 = \frac{2qf_L I_{B1}^{\gamma}}{f} \tag{4.117}$$

$$I_{fib2}^2 = \frac{2qf_L I_{B2}^{\gamma}}{f} \tag{4.118}$$

$$E_{RC3}^2 = 4kTR_{C3} \tag{4.119}$$

$$E_{RC4}^2 = 4kTR_{C4} \tag{4.120}$$

$$E_{rx3}^2 = 4kTr_{x3} \tag{4.121}$$

$$E_{rx4}^2 = 4kTr_{x4} \tag{4.122}$$

$$I_{sic3}^2 = 2qI_{C3} \tag{4.123}$$

$$I_{sic4}^2 = 2qI_{C4} \tag{4.124}$$

$$I_{sib3}^2 = 2qI_{B3} \tag{4.125}$$

$$I_{sib4}^2 = 2qI_{B4} \tag{4.126}$$

$$I_{fib3}^2 = \frac{2qf_L I_{B3}^{\gamma}}{f} \tag{4.127}$$

$$I_{fib4}^2 = \frac{2qf_L I_{B4}^{\gamma}}{f} \tag{4.128}$$

The noise contributions of the current sources at their outputs are obtained from Section 4.3.1. The equations for the noise contributions of the instrumentation amplifier at its output are as given in Section 4.3.2. Since the output of the instrumentation amplifier is the output of the full LNA design, these equations do not undergo any additional adjustments. The noise contributions of the differential amplifier noise sources at the output of the instrumentation amplifier (v_{out}) are given below.

Thermal noise contributions of the first differential amplifier at v_{out}:

$$E_{oRB1}^2 = E_{RB1}^2 \times A_{d1}^2 \times A_{d2}^2 \times A_{vi}^2 \tag{4.129}$$

$$E_{oRB2}^2 = E_{RB2}^2 \times A_{d1}^2 \times A_{d2}^2 \times A_{vi}^2 \tag{4.130}$$

$$E_{oRC1}^2 = E_{RC1}^2 \times (\frac{R_{in3}||r_{o1}}{R_{in3}||r_{o1} + R_{C1}})^2 \times A_{d2}^2 \times A_{vi}^2 \tag{4.131}$$

$$E_{oRC2}^2 = E_{RC2}^2 \times (\frac{R_{in4}||r_{o2}}{R_{in4}||r_{o2} + R_{C2}})^2 \times A_{d2}^2 \times A_{vi}^2 \tag{4.132}$$

$$E_{orx1}^2 = E_{rx1}^2 \times (\frac{2r_{\pi 1}}{2r_{\pi 1} + r_{x1} + R_{B1}})^2 \times A_{d1}^2 \times A_{d2}^2 \times A_{vi}^2 \tag{4.133}$$

$$E_{orx2}^2 = E_{rx2}^2 \times (\frac{2r_{\pi 2}}{2r_{\pi 2} + r_{x2} + R_{B2}})^2 \times A_{d1}^2 \times A_{d2}^2 \times A_{vi}^2 \tag{4.134}$$

Since the values of R_{B1} and R_{B2} are so small (5 Ω), the calculation of the equivalent output noise due to their contribution is simplified from the equation in Section 4.3.3.

Shot noise contributions of the first differential amplifier at v_{out}:

$$E_{osic1}^2 = I_{sic1}^2 \times (R_{C1}||r_{o1}||R_{in3})^2 \times A_{d2}^2 \times A_{vi}^2 \tag{4.135}$$

$$E_{osic2}^2 = I_{sic2}^2 \times (R_{C2}||r_{o2}||R_{in4})^2 \times A_{d2}^2 \times A_{vi}^2 \tag{4.136}$$

$$E_{osib1}^2 = I_{sib1}^2 \times ((R_{B1} + r_{x1})||(2r_{\pi 1}))^2 \times A_{d1}^2 \times A_{d2}^2 \times A_{vi}^2 \tag{4.137}$$

$$E_{osib2}^2 = I_{sib2}^2 \times ((R_{B2} + r_{x2})||(2r_{\pi 2}))^2 \times A_{d2}^2 \times A_{d2}^2 \times A_{vi}^2 \tag{4.138}$$

Flicker noise contributions of the first differential amplifier at v_{out}:

$$E_{ofib1}^2 = I_{fib1}^2 \times ((R_{B1} + r_{x1})||(2r_{\pi 1}))^2 \times A_{d1}^2 \times A_{d2}^2 \times A_{vi}^2 \tag{4.139}$$

$$E_{ofib2}^2 = I_{fib2}^2 \times ((R_{B2} + r_{x2})||(2r_{\pi 2}))^2 \times A_{d2}^2 \times A_{d2}^2 \times A_{vi}^2 \tag{4.140}$$

Thermal noise contributions of the second differential amplifier at v_{out}:

$$E_{oRC3}^2 = E_{RC3}^2 \times (\frac{r_{o3}}{r_{o3} + R_{C3}})^2 \times A_{vi}^2 \tag{4.141}$$

$$E_{oRC4}^2 = E_{RC4}^2 \times (\frac{r_{o4}}{r_{o4} + R_{C4}})^2 \times A_{vi}^2 \tag{4.142}$$

$$E_{orx3}^2 = E_{rx3}^2 \times (\frac{2r_{\pi 3}}{2r_{\pi 3} + r_{x3} + R_{C1}})^2 \times A_{vi}^2 \tag{4.143}$$

$$E_{orx4}^2 = E_{rx4}^2 \times (\frac{2r_{\pi 4}}{2r_{\pi 4} + r_{x4} + R_{C2}})^2 \times A_{vi}^2 \tag{4.144}$$

Shot noise contributions of the second differential amplifier at v_{out}:

$$E_{osic3}^2 = I_{sic3}^2 \times (R_{C3}||r_{o3})^2 \times A_{vi}^2 \tag{4.145}$$

$$E_{osic4}^2 = I_{sic4}^2 \times (R_{C4}||r_{o4})^2 \times A_{vi}^2 \tag{4.146}$$

$$E_{osib3}^2 = I_{sib3}^2 \times ((R_{C1} + r_{x3})||(2r_{\pi 3}))^2 \times A_{d2}^2 \times A_{vi}^2 \tag{4.147}$$

$$E_{osib4}^2 = I_{sib4}^2 \times ((R_{C2} + r_{x4})||(2r_{\pi 4}))^2 \times A_{d2}^2 \times A_{vi}^2 \tag{4.148}$$

Flicker noise contributions of the second differential amplifier at v_{out}:

$$E_{ofib3}^2 = I_{fib3}^2 \times ((R_{C1} + r_{x3})||(2r_{\pi 3}))^2 \times A_{d2}^2 \times A_{vi}^2 \tag{4.149}$$

$$E_{ofib4}^2 = I_{fib4}^2 \times ((R_{C2} + r_{x4})||(2r_{\pi 4}))^2 \times A_{d2}^2 \times A_{vi}^2 \tag{4.150}$$

Noise contribution of the first current source at v_{out}:

$$E_{oco1}^2 = E_{co1}^2 \times A_{cd1}^2 \times A_{d2}^2 \times A_{vi}^2 \tag{4.151}$$

Noise contribution of the second current source at v_{out}:

$$E_{oco2}^2 = E_{co2}^2 \times A_{cd2}^2 \times A_{vi}^2 \tag{4.152}$$

Simulation Results:

Two types of hand calculations were performed for the multistage differential amplifier design. The first set of calculations used the following assumptions to calculate small signal parameters and circuit gains

$$\beta_1 = \beta_2 = \beta_3 = \beta_4 = \beta_{c1} = \beta_{c2} = \beta_{c3} = \beta_{c4} = 500$$
$$I_{cc1} = I_{cc2} = I_{cc3} = I_{cc4} = 2I_{c1} = 2I_{c2} = 2I_{c3} = 2I_{c4}.$$

The second set of calculations aimed to provide a more accurate view of the circuit noise since the first set did not adequately account for the noise of the second current source. For the more accurate calculations the simulated collector and base currents of each transistor were obtained from LTspice and used to determine the small signal transistor parameters and β values for the circuit. Additionally, the simulated gains A_{d1} and A_{d2} were obtained directly from the Spice simulation.

Once again, the hand calculations and simulation used $R_{C2} = R_{C1} \times 1.0001$ to account for the effect of mismatched resistors on circuit noise.

The equivalent input noise for the different I_C designs was calculated by dividing the total equivalent output noise by the full gain ($A_{d1} \times A_{d2} \times A_{vi}$). The results obtained from both sets of hand calculations were then plotted using MATLAB so that they could be directly compared with the equivalent input noise graphs obtained from simulation.

As with single stage differential amplifier design, it is important to note that all of the results include the effect of the thermal noise in resistors R_{B1} and R_{B2}. Since these resistors are a

representation of the resistance of the SQUID after the transformer, they don't contribute thermal noise to the equivalent input noise of the amplifier. Since the resistor values are so small they do not contribute much noise to the flatband region, but the equivalent input noise of each amplifier in the flatband is still slightly lower than the plots indicate. Since the resistors contribute the same thermal noise for each design, a fair comparison of the three designs could be made without removing the noise contribution of R_{B1} and R_{B2}.

Tables D.4, D.5 and D.6 in Appendix D contain a comparison of the output noise contributions of every noise source in the circuit when I_C of the differential amplifier is chosen as 500 μA, 1mA and 2 mA respectively. The tables include results obtained from both types of hand calculation as well as those from simulation.

Figures 4.25, 4.27 and 4.29 show the plots of equivalent input noise and gain magnitude obtained from simulation for $I_C = 500$ μA, 1 mA and 2 mA respectively. Figures 4.26, 4.28 and 4.30 show the plot of equivalent input noise obtained via both type of hand calculations for $I_C = 500$ μA, 1 mA and 2 mA respectively.

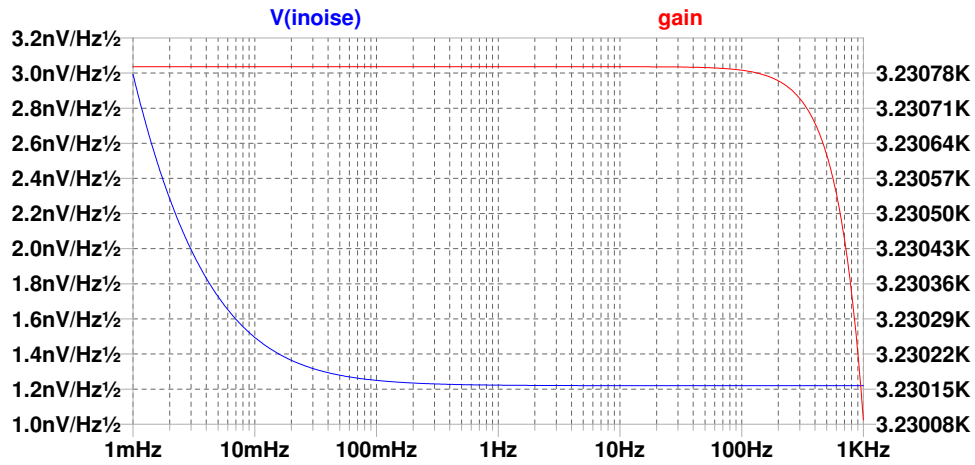


Figure 4.25: Simulation results showing the gain and equivalent input noise when I_C is chosen as 500 μA for a multistage differential amplifier design.

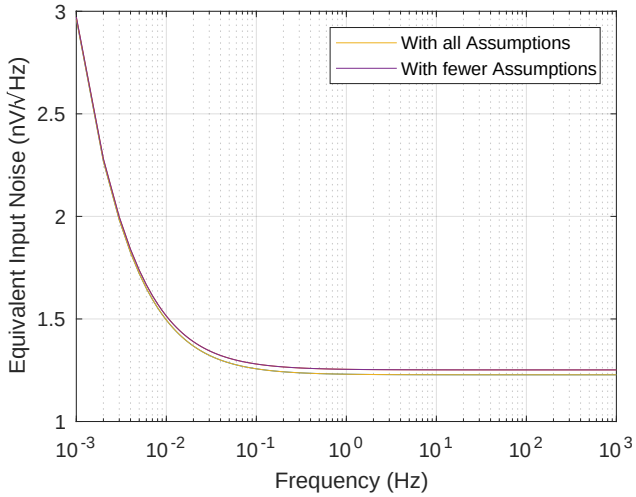


Figure 4.26: Hand calculation results showing the equivalent input noise when I_C is chosen as 500 μA for a multistage differential amplifier design.

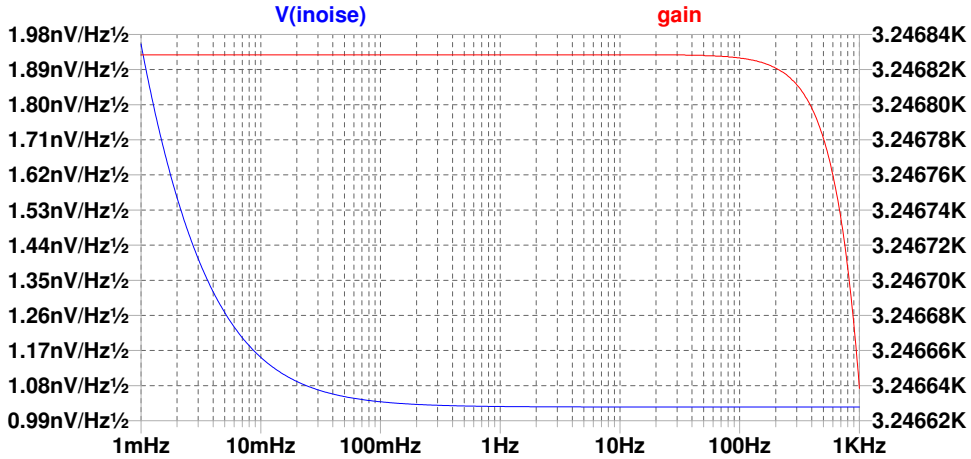


Figure 4.27: Simulation results showing the gain and equivalent input noise when I_C is chosen as 1 mA for a multistage differential amplifier design.

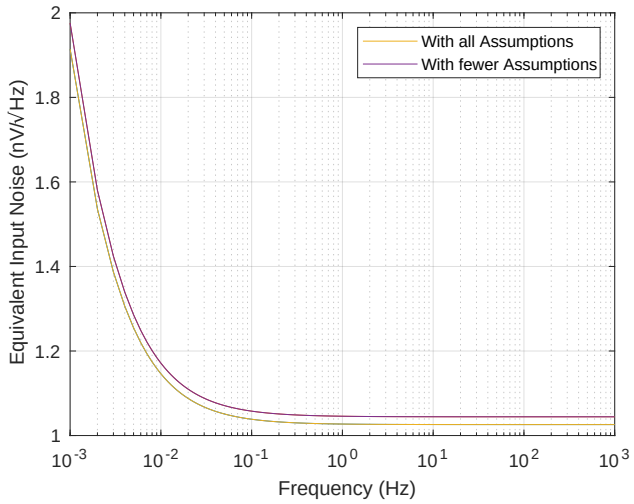


Figure 4.28: Hand calculation results showing the equivalent input noise when I_C is chosen as 1 mA for a multistage differential amplifier design.

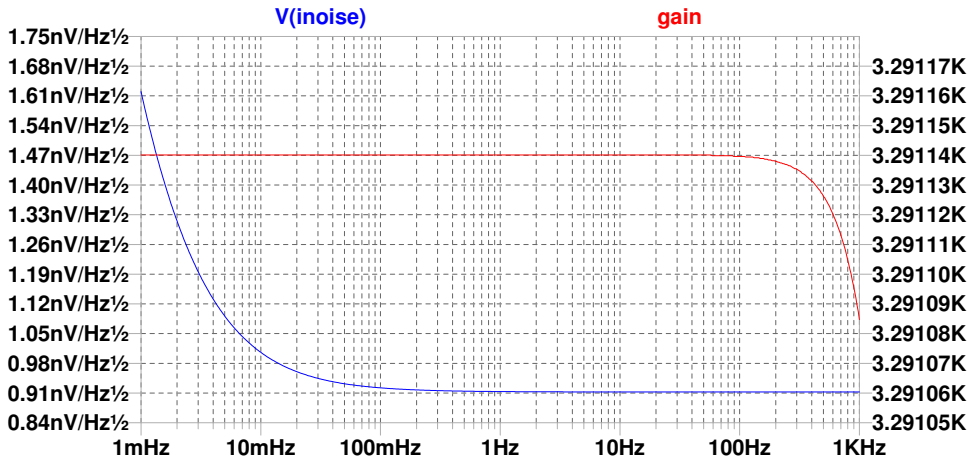


Figure 4.29: Simulation results showing the gain and equivalent input noise when I_C is chosen as 2 mA for a multistage differential amplifier design.

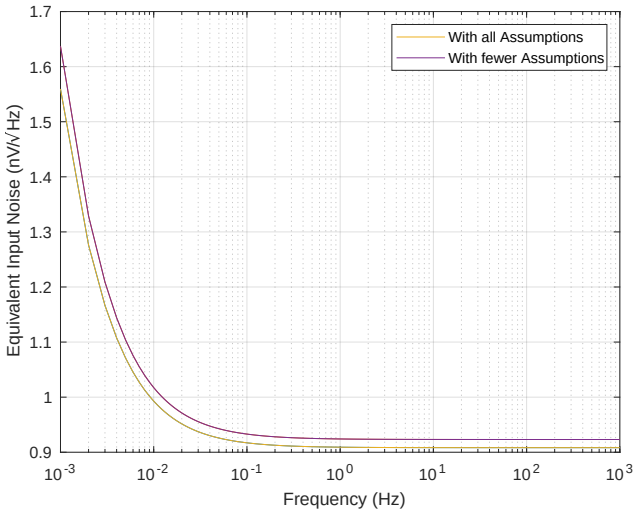


Figure 4.30: Hand calculation results showing the equivalent input noise when I_C is chosen as 2 mA for a multistage differential amplifier design.

Table 4.6 contains a summary of the calculated and simulated equivalent input noise results for each of the three I_C values. Calc. 1 is the hand calculations with all assumptions while Calc. 2 uses the current and gain values obtained from simulation.

Table 4.6: Summary of the noise response of the multistage differential amplifier pre-amplifier for each I_C value

	500 μA			**1 mA**			**2 mA**		
	Calc. 1	**Calc. 2**	**Sim.**	**Calc. 1**	**Calc. 2**	**Sim.**	**Calc. 1**	**Calc. 2**	**Sim.**
Flatband Noise ($\mathbf{nV/\sqrt{Hz}}$)	1.228	1.252	1.220	1.026	1.044	1.025	0.908	0.923	0.912
Nosie at 1 mHz ($\mathbf{nV/\sqrt{Hz}}$)	2.963	2.972	2.993	1.914	1.976	1.956	1.560	1.637	1.620

Both sets of hand calculations correspond well with the simulation results. Since the R_C values in this design are small and the combined gain of the two differential stages is high, the flicker noise contribution of the operational amplifier's current noise has very little effect on the full LNA noise.

Once again, the design that used $I_C = 2$ mA produced the best noise results for both the flatband and flicker noise regions. Since the optional transformer is not included in this design, the noise is not further attenuated at the input of the SQUID. This design has a better flicker noise response than the single stage differential amplifier LNA, but worse flatband noise.

An attempt was made to adjust this circuit design to include the optional transformer by dropping the gain of the first differential amplifier. The transformer cannot be included without dropping the gain due to the risk of the SQUID offset voltage driving the output to clip.

The collector current of the differential amplifier transistors was chosen as $I_{C1} = 1$ mA and the collector resistors of the first differential amplifier were set to $R_{C1} = R_{C2} = 780\ \Omega$. Theoretically

this would have produced a differential gain close to $A_{d1} = -30$ for the first differential amplifier stage. Once the circuit was simulated, however, the gain was far lower than expected. Figure 4.31 shows the magnitude of the gains at the output of the instrumentation amplifier (V(out)), the output of the second differential amplifier stage (V(nC4,nC3)) and the output of the first differential amplifier stage (V(nC2,nC1)).

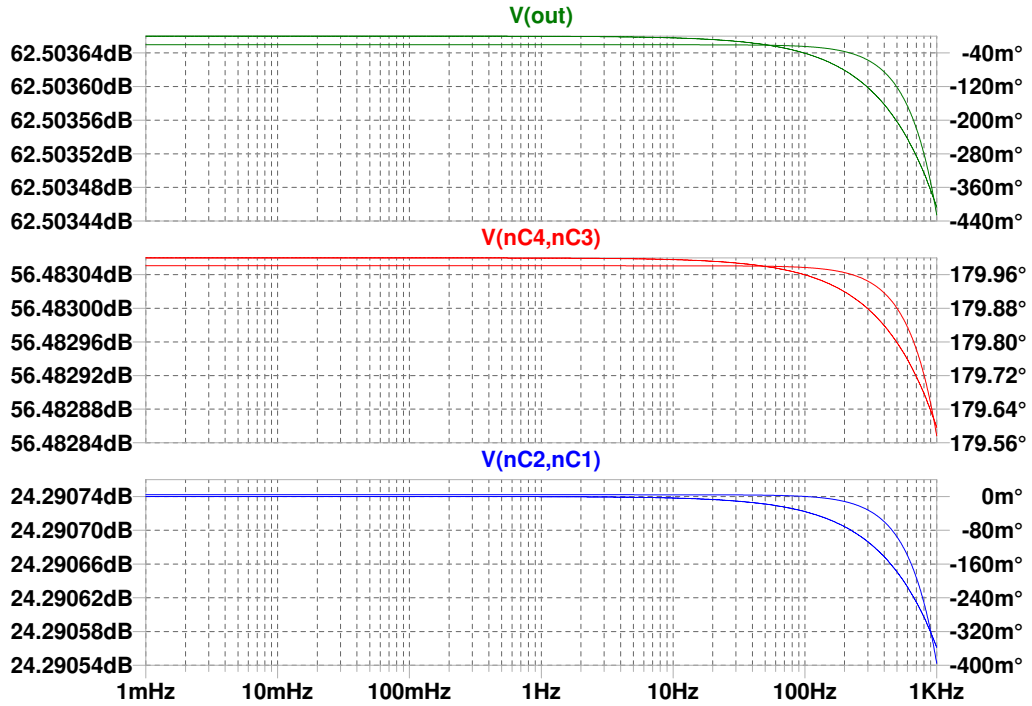


Figure 4.31: Gain for a multistage differential amplifier pre-amplifier with the gain of the first stage lowered.

The gain of the first differential stage was simulated as $|A_{d1}| = 16.389$. Even accounting for the expected input resistance of the second stage, this gain was far lower than expected.

A closer examination of the DC characteristics of the circuit revealed the reason for this drop in gain. A smaller collector resistance in the first differential amplifier resulted in a large DC offset at the collectors of Q1 and Q2. The larger collector resistance in the second differential amplifier produced a smaller DC offset at the collectors of Q3 and Q4. Since the collectors of Q1 and Q2 were connected to the bases of Q3 and Q4 respectively, this means that the voltage at the bases of Q3 and Q4 is higher than the voltage at their collectors at the operating point. As a result, the transistors in the second differential amplifier are driven into saturation, and the input resistance of the second stage is far lower than originally calculated.

Once the reason for this issue was determined, the DC characteristics of the design with $A_{d1} = A_{d2}$ were checked by simulation. Once again, the voltage at the bases of Q3 and Q4 was higher than at their collectors. In this case, the difference in voltage was very small (around 0.03 V). As a result, the transistors were not driven into their hard saturation stage, but into a region known as quasi-saturation. In this region, there is still some relation between I_B and I_C of the transistor, but the constant β relation is no longer applicable. In addition, the collector and base resistances of the transistor are smaller than for a transistor in the normal active region [45].

The transistor model for the SSM2212 doesn't contain the necessary parameters to model the

transistor in its quasi-saturation region. As a result, the results obtained by simulation for the two stage differential amplifier with $A_{d1} = A_{d2}$ can't be considered an accurate representation of the actual circuit response.

This situation could be avoided by choosing $R_{C1} = R_{C2}$ larger than $R_{C3} = R_{C4}$, but this would increase the gain of the first stage and lead to an increased probability of the voltage clipping in the second stage due to the SQUID offset voltage.

As a result, the multistage differential amplifier is not a suitable option for the pre-amplifier of the FLL despite its good flicker noise response.

4.4 Selected Design

Of the three pre-amplifier options considered in Sections 4.2, 4.3.3 and 4.3.4, the single stage differential amplifier had the fewest design flaws. The biggest problem with this design was the large flicker noise response caused by the current noise of the LT1028 operational amplifiers in the instrumentation amplifier stage. For the selected pre-amplifier design, the single stage differential amplifier circuit configuration with optional transformer is used, but a different operational amplifier is chosen for the instrumentation amplifier stage.

The LT1028 used in the initial designs has a typical voltage noise of 1 nV/$\sqrt{\text{Hz}}$ in the flatband and a corner frequency of 3.5 Hz. The typical value of the current noise is 1 pA/$\sqrt{\text{Hz}}$ in the flatband with a corner frequency of 250 Hz (worst case 1.8 pA/$\sqrt{\text{Hz}}$ with corner frequency of 800 Hz) [34].

The LT1007 from Analog Devices was chosen as a suitable replacement. It has a typical voltage noise of 2.5 nV/$\sqrt{\text{Hz}}$ in the flatband and a corner frequency of 2 Hz. The typical value of the current noise is 0.4 pA/$\sqrt{\text{Hz}}$ in the flatband with a corner frequency of 120 Hz (worst case 0.6 pA/$\sqrt{\text{Hz}}$ with corner frequency of approximately 600 Hz) [32]. The improved current noise characteristics with lower corner frequency are what makes the LT1007 a desirable replacement.

Since the noise contribution of the operational amplifier's current noise increases with decreasing I_C (increasing R_C) and the flicker noise contribution of the transistors increases with increasing I_C, the chosen I_C value needed to be a compromise between these two noise contributions. As such, the collector current of the differential amplifier transistors was chosen as $I_C = 1$ mA.

The calculations from Section 4.3.3 were repeated with the new noise characteristics for the operational amplifier. Table 4.7 contains the calculated and simulated noise contribution at the output for each noise source.

Table 4.7: Comparison of calculated and simulated noise for each noise source in a single stage differential amplifier with $I_{C1} = I_{C2} = 1$ mA using the LT1007 operational amplifier.

	Noise Source	**1 mA**	
		Hand Calculation	**Spice Simulation**
Differential Amplifier	R_{B1}	524.254 n	518.378 n
	R_{B2}	524.254 n	518.378 n
	R_{C1}	17.850 n	17.244 n
	R_{C2}	17.851 n	17.245 n
	rx1	168.982 n	167.172 n
	rx2	168.982 n	167.172 n

	sic1	166.741 n	167.194 n
	sic2	166.757n	167.195 n
	sib1/fib1	40.208 n	42.341 n
	sib2/fib2	40.208 n	42.342 n
Current Source	R_1	0.899 p	0.860 p
	rcx1	17.017 p	15.942 p
	rcx2	17.065 p	15.991 p
	sicc1	12.062 p	11.321 p
	sicc2	12.144 p	11.251 p
	sibc1/fibc1	0 p	0.002 p
	sibc2/fibc2	1.080 p	1.088 p
Instrumentation Amplifier	All R_A	1.287 n	1.288 n
	R_{GAIN}	1.820 n	1.821 n
	En1	5.00 n	NA
	En2	5.00 n	NA
	En3	5.00 n	NA
	Enf1	6.325 n	NA
	Enf2	6.325 n	NA
	Enf3	6.325 n	NA
	In1	3.848 n	NA
	In2	3.848 n	NA
	In3	40.000 p	NA
	Inf1	45.636 n	NA
	Inf2	45.636 n	NA
	Inf3	9.487 p	NA
TOTAL FLATBAND NOISE		**816.3 nV/$\sqrt{\text{Hz}}$**	**808.3 nV/$\sqrt{\text{Hz}}$**
TOTAL FLICKER NOISE		**86.7 nV/$\sqrt{\text{Hz}}$**	**NA**

Figure 4.32 shows the simulated equivalent input noise and gain with $I_C = 1$ mA. The simulated flatband noise is 2.240 nV/$\sqrt{\text{Hz}}$ and the noise at 1 mHz is 7.732 nV/$\sqrt{\text{Hz}}$. Figure 4.33 pn the next page shows the calculated equivalent input noise for $I_C = 1$ mA. The flatband noise is calculated at 2.230 nV/$\sqrt{\text{Hz}}$ and the noise at 1 mHz is calculated as 7.843 nV/$\sqrt{\text{Hz}}$.

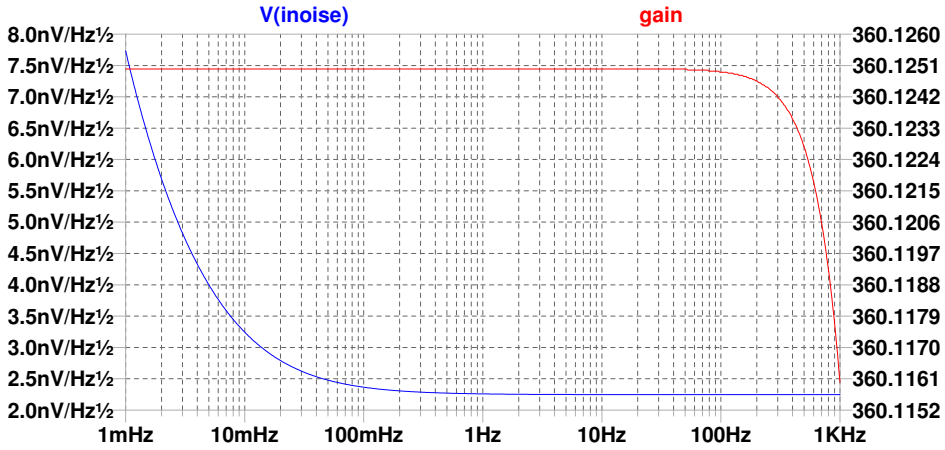


Figure 4.32: Simulation results showing the gain and equivalent input noise when I_C is chosen as 1 mA for a single stage differential amplifier design using the LT1007 operational amplifier.

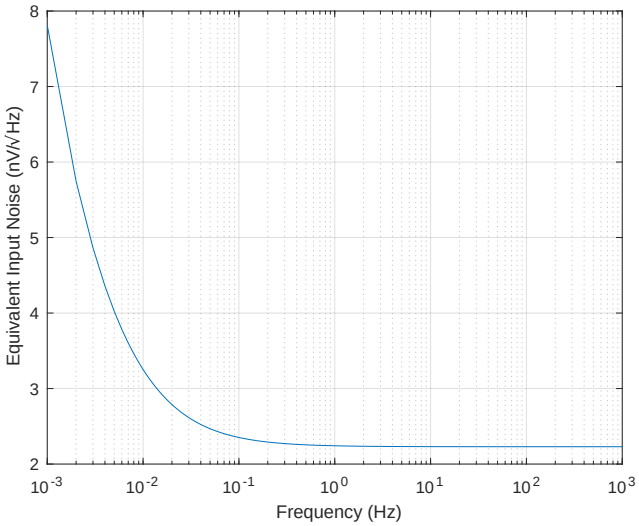


Figure 4.33: Hand calculation results showing the equivalent input noise when I_C is chosen as 1 mA for a single stage differential amplifier design using the LT1007 operational amplifier.

The noise response of the circuit is extremely promising with a very low corner frequency (approximately 6 mHz from simulation) and a reasonable level of flicker noise. Since resistors R_{B1} and R_{B2} just represent the source resistance of the SQUID, they do not contribute thermal noise to the circuit. To account for this, the circuit was simulated again, with the resistors R_{B1} and R_{B2} set as noiseless resistors. Figure 4.34 on the next page shows the equivalent input noise of the pre-amplifier as seen after the transformer.

The simulated flatband noise is then 0.951 nV/$\sqrt{Hz}$ and the noise at 1 mHz is 7.466 nV/$\sqrt{Hz}$. This is the equivalent input noise of the pre-amplifier after the transformer. To determine the equivalent input noise of the pre-amplifier at the SQUID, this value still needs to be divided by five (5:1 turns ratio on the SQUID). The final noise results for the pre-amplifier are then:

Flatband Noise:	0.190 nV/$\sqrt{\text{Hz}}$
Noise at 1 mHz:	1.493 nV/$\sqrt{\text{Hz}}$
Corner Frequency f_C:	6 mHz

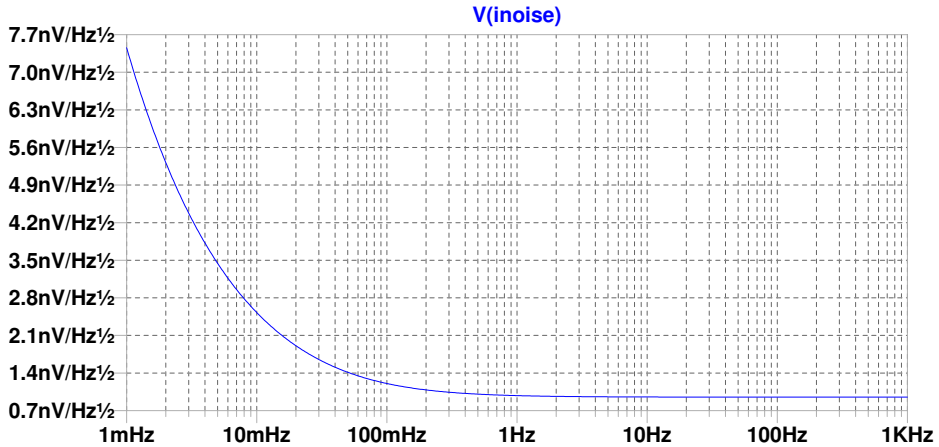


Figure 4.34: Simulation results showing the equivalent input noise of the selected pre-amplifier design after the transformer.

4.5 Summary of Pre-amplifier Designs

Table 4.8 contains a summary of the most promising pre-amplifier designs from this chapter. The Opamp column indicates which operational amplifier was used for the secondary amplifier in the common emitter design and the instrumentation amplifier in the differential amplifier designs. The transformer (Trans.) column indicates whether or not the pre-amplifier would use the optional transformer from the M2700 magnetometer package. I_C is the selected current for the single transistor in the common emitter design and the differential amplifier transistors in the differential designs. Gain is the full gain of the pre-amplifier stage from the SQUID to the output (including transformer as required). The table also provides an indication of the equivalent input noise contribution of the circuit at the SQUID for both the flatband region and at 1 mHz. The gain and noise values were obtained from simulation. The last column includes a summary of the major identified design flaws in the pre-amplifier designs.

Table 4.8: Summary of the best pre-amplifier designs from Chapter 4.

Design	Opamp	Trans.	I_C	Gain	Noise ($V/\sqrt{Hz}$)	Design Flaws
Common Emitter	LT1028	NA	1 mA	341	Flat: 1.61 n 1 mHz: 4.81 μ	Long Settling Time Very Poor $1/f$ Response
Single Stage Differential	LT1028	Y	2 mA	1800	Flat: 0.17 n 1 mHz: 4.98 n	Opamp $1/f$ response
Two Stage Differential	LT1028	N	2 mA	3290	Flat: 0.82 n 1 mHz: 1.97 n	Quasi-Saturation SQUID Offset Voltage
Single Stage Differential	LT1007	Y	1 mA	1800	Flat: 0.19 n 1 mHz: 1.49 n	-

This table provides a clear indication that the single stage differential designs are the most suitable since they lack the major design flaws of the two stage differential and common emitter designs. The design with the LT1007 operational amplifier has the best $1/f$ noise performance, whereas the design with the LT1028 operational amplifier has the best flatband noise performance due to the lower R_C values. The difference in the flatband noise between the two designs is very small, so the design using the LT1007 is the more suitable design due to its excellent $1/f$ noise performance. As such, it was the chosen design for the proposed FLL.

4.6 Secondary Amplification and Voltage Offset Removal

When a SQUID is biased with a current, it has an offset voltage about which the voltage swings. When bias current reversal is used, this voltage offset switches positive and negative at the same frequency as the bias reversal current. Since the voltage offset is normally considerably larger than the desired SQUID output, the desired signal is masked by the square-wave switching offset.

In some systems like the one in [4], the voltage offset is removed before the pre-amplifier. One issue with this method, is that the system used to supply the voltage offset has to be extremely low noise since the noise would be added directly to the SQUID. The alternative considered in this research involves removing the voltage offset during a secondary amplification stage after the initial pre-amplifier. By doing this, the noise of the voltage offset removal system is attenuated by the gain of the pre-amplifier.

Since the pre-amplifier stage has a gain of -360, the offset voltage contribution after the pre-amplifier stage has the same frequency as the SQUID bias current, but is phase-shifted by 180°. If an appropriate square-wave voltage is summed with the output voltage from the pre-amplifier, the voltage offset would be cancelled out.

Figure 4.35 shows the circuit used for secondary amplification and voltage offset removal.

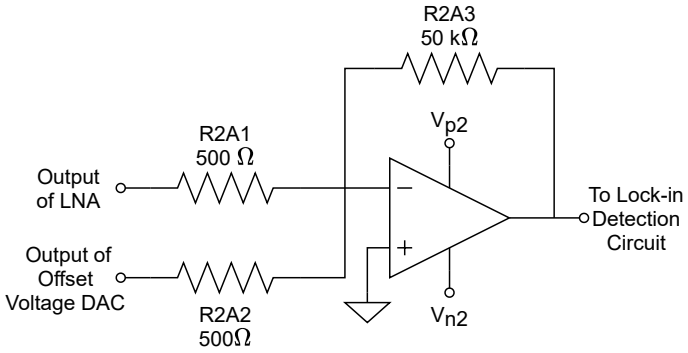


Figure 4.35: Circuit diagram of the secondary amplification stage with voltage offset removal.

The secondary amplifier consists of an inverting summing operational amplifier circuit with a gain of $A_{VSA} = -100$. The circuit sums the output from the pre-amplifier stage and the signal used to remove the voltage offset. Since the output of the pre-amplifier due to the voltage offset is a square wave with the same frequency but a 180° phase shift from the bias current, a square wave voltage with the same frequency that is in-phase with the bias current is required.

The DAC8812 that was used to provide the bias reversal and flux modulation currents can be used to provide the signal required for voltage offset removal. If an operational amplifier is used at the output of the DAC8812, it converts the output current to a voltage as discussed in Section 3.3.3. The voltage output of this operational amplifier is then

$$V_{out} = V_{REF} \times \frac{D}{65536}$$

If the same reference signal used for producing the bias current is used to produce the voltage offset, then a square-wave voltage with the required frequency and phase can be obtained. Considering this reference switches between 5 V and -5 V, the minimum voltage increment at the output is then 76 μV. This does not provide fine enough control over the output voltage to counter the voltage offset. A simple resistor division circuit can be used to drop the voltage of the reference signal to so that it switches between approximately 500 mV and -500 mV. For this voltage reference, the minimum voltage increment of the DAC is 7.6 μV which is acceptable.

The DAC8812 can be controlled in the same way as discussed in Section 3.3.3.

Chapter 5

FLL Simulations

Once the FLL design process was complete, the full system was analysed and adjusted to improve the noise response. Thereafter, the FLL was simulated in LTspice to determine if the design was successful.

This chapter discusses the closed-loop FLL bandwidth (f_{-3dB}) and refinements made to the design to improve the noise response. It also considers the method used to simulate the SQUID, accounting for bias current reversal, flux modulation and the optional transformer. Afterwards, the simulation of the complete FLL is discussed and the simulation results are analysed.

5.1 FLL Bandwidth and Noise Considerations

From [3], the equation to calculate the closed-loop bandwidth of the FLL is given by

$$f_{-3dB} = \frac{G \times \delta V/\delta\Phi_0 \times f_{INT}}{R_f/M_f} \tag{5.1}$$

where G is the combined gain of the amplification stages in the FLL between the SQUID and the integrator. This gain includes the effect of the optional transformer.

$$G = A_d \times A_{vi} \times A_{VSA} \times 5 \tag{5.2}$$

$\delta V/\delta\Phi_0$ is the transfer function of the SQUID, f_{INT} is the frequency of the integrator, R_f is the feedback resistor and $1/M_f$ is the feedback mutual inductance of the SQUID. For the considered FLL design using the M2700 we have

$$\begin{gathered} \text{G} = 180000 \\ \delta V/\delta\Phi_0 = 60\ \mu\text{V}/\Phi_0 \\ f_{INT} = 1/2\pi\tau \text{ with } \tau = 20\ \mu\text{s, } 200\ \mu\text{s or } 2\text{ ms} \\ R_f = 600\ \text{k}\Omega\text{, } 60\ \text{k}\Omega \text{ or } 6\ \text{k}\Omega \\ 1/M_f = 17\ \mu\text{A}/\Phi_0 \end{gathered}$$

The capacitors from Section 3.5 were chosen such that their effect on the closed-loop bandwidth of the FLL would be the same for all three calibration factors.

The closed-loop bandwidth of the designed FLL for the M2700 is calculated as $f_{-3dB} = 8.426$ kHz. According to [1], the noise bandwidth of a FLL for a first-order low pass response is

approximated as

$$\Delta f = \frac{\pi}{2} f_{-3dB} \tag{5.3}$$

For the proposed FLL design, the noise bandwidth is then $\Delta f = 13.236$ kHz.

To calculate the RMS noise contribution of sections of a system, the noise voltage density is integrated over the noise bandwidth [14]. This means that a reduced noise bandwidth corresponds with less RMS noise. In order to decrease the noise bandwidth of the FLL, the closed-loop bandwidth needs to be decreased. Since the focus of the FLL design is on ultra-low-frequency measurements, a bandwidth of $f_{-3dB} = 8.426$ kHz is higher than actually required and can be lowered without impacting the FLL performance in the region of interest.

The simplest way to decrease the system bandwidth is to increase the value of the integrator capacitors from Section 3.5 without changing any other values. This will increase the integration time and decrease the crossover frequency of the integrator. New integrator capacitor values that are 2.5 times larger are chosen. Table 5.1 contains the updated integrator capacitors and corresponding time constants for each feedback resistor and calibration factor.

Table 5.1: Updated integrator capacitor values with corresponding feedback resistors.

Feedback Resistor	Calibration Factor	Full-scale Range	Integration Time	Integrator Capacitor	Integrator Resistor
600 kΩ	10.2 V/Φ_0	1.96Φ_0	50 μs	5 nF	
60 kΩ	1.02 V/Φ_0	19.6Φ_0	500 μs	50 nF	10 kΩ
6 kΩ	102 mV/Φ_0	196Φ_0	5 ms	500 nF	

For these capacitor values, the new system bandwidth is calculated as $f_{-3dB} = 3.370$ kHz. The corresponding noise bandwidth is then $\Delta f = 5.294$ kHz. LTspice allows the user to integrate the equivalent input noise of a circuit over a specified noise bandwidth. The noise contribution of the pre-amplifier was determined by integrating the equivalent input noise before the transformer determined in Section 4.4, over the region from 1 nHz to 5.294 kHz. The value of 1 nHz was chosen as a suitably low frequency to provide a good view of the RMS noise voltage. Theoretically, the 1/f noise increases infinitely with decreasing frequency, but practical aspects of circuits prevent the RMS noise from actually being infinite [14]. An RMS noise voltage of 13.846 nV_{RMS} was calculated for the pre-amplifier.

5.2 Simulated SQUID

Figure 5.1 on the next page shows the LTspice schematic used to simulate the M2700 SQUID with flux modulation, bias current reversal and the optional transformer. The Digital Phase Splitter and current output DACs were not included in the schematic in order to simplify the circuit and keep the simulation times low enough to effectively evaluate the full FLL at low frequencies. Instead, current sources were used to represent the flux modulation and bias currents of the FLL.

Since the SQUID is modelled on the ideal parameters of the M2700 from Section 2.3, the modulation current, bias current and applied flux were chosen accordingly.

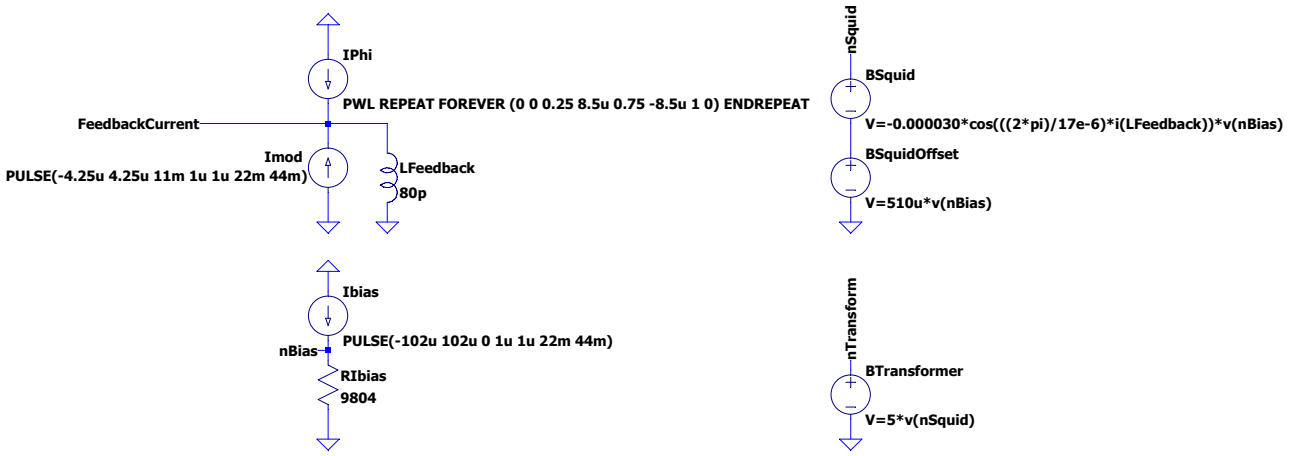


Figure 5.1: LTspice model of the M2700 SQUID including bias current reversal, flux modulation and the optional transformer.

Iphi represents the current used to apply a test input magnetic flux to the modelled SQUID. In an actual FLL, this current would be applied to the feedback coil of the SQUID to induce a magnetic field in the SQUID's pickup loop. The value of Iphi is chosen according to the feedback mutual inductance of the particular SQUID. For the M2700 this value is 17 μA/Φ_0. As discussed in Section 3.5, a triangular input flux corresponding to $1\Phi_0$ in the SQUID loop would be chosen for tuning (open-loop operation) of the FLL. As such, the peak-to-peak current chosen for the Iphi is 17 μA.

Ibias represents the bias reversal current through the SQUID. Since this current is not actually processed through the LTspice model of the SQUID, it is just represented as a current through a resistor. As discussed in Section 3.3, a square-wave bias current that switches from 102 μA to -102 μA is suitable. The resistor is chosen such that the voltage across it is approximately equal to $\pm$ 1 V as the bias current switches. For an assumed Arduino PWM output frequency of 45 Hz, the bias reversal frequency was chosen as approximately 22.5 Hz (actual frequency for the simulation was closer to 22.7 Hz).

Imod represents the modulation current through the feedback coil that is used to apply flux modulation to the SQUID. As discussed in Section 3.3, the flux modulation current is chosen as a square-wave signal with a peak-to-peak value corresponding with an applied flux of $\Phi_0/2$. Imod is therefore represented as a pulsed source with a current that periodically switches between 4.5 μA and -4.5 μA. For an assumed Arduino PWM output frequency of 45 Hz, the frequency of the square-wave current Imod is chosen as approximately 22.5 Hz (actual frequency for the simulation was closer to 22.7 Hz). Since the flux modulation current is designed to be 90° phase-shifted from the bias current, a delay equal to one quarter of the period is added to Imod.

The current from Imod was summed with the current from IPhi. The resulting current was passed through an inductor. This inductor has no impact on any of the simulated values and is just used a representation of the feedback coil. The BSquid voltage source that was used to model the SQUID in section 2.4, calculates the theoretical voltage output of the SQUID from the current through the inductor "feedback coil". The polarity of this calculated output was switched at the same frequency as Ibias by multiplying the calculated output by the voltage over the bias current resistor ($\pm$1 V). The voltage offset of the SQUID was included as a voltage source of 510 μV that also switched polarity with Ibias. Another voltage source, BTransformer, was used to calculate the total SQUID voltage after the optional transformer by multiplying the

combined output of BSquid and the voltage offset source by 5.

Figure 5.2 shows the simulated outputs of the different sources in the schematic. The rise and fall times for the square-wave signals were assumed as 1 μs for simplification purposes.

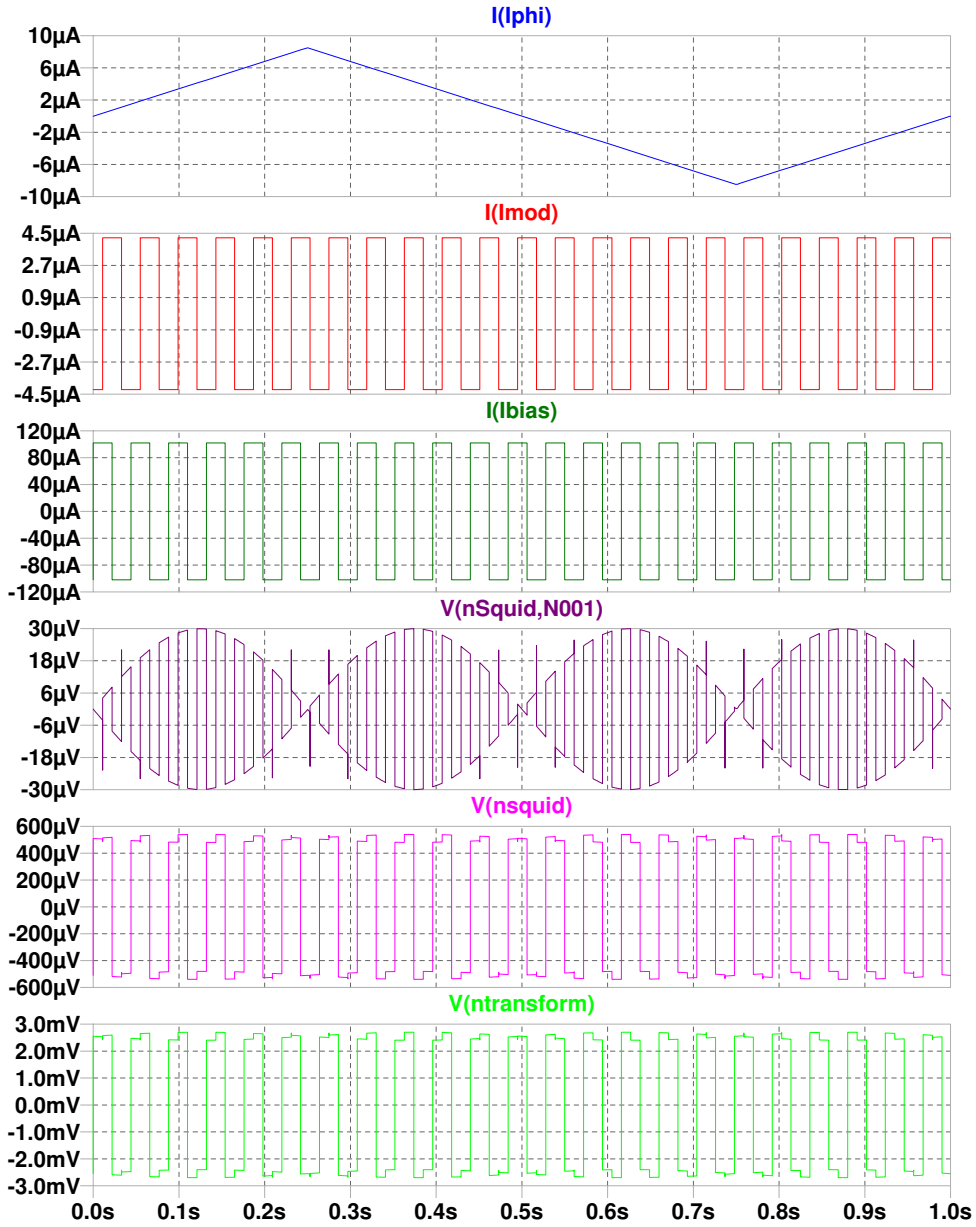


Figure 5.2: Simulated outputs for the full LTspice model of the M2700 SQUID including bias current reversal, flux modulation and the optional transformer.

5.3 FLL Simulation

The full FLL design was simulated using the schematic included in Appendix E which shows the FLL in open-loop configuration. As with the flux modulation and bias currents, the Arduino PWM output and the square-wave voltage used for offset removal were implemented as simple square-wave voltage sources with fall and rise times of 1 μs. The amplitude of the Arduino PWM output switched between 0 V and 5 V with a frequency of approximately 45 Hz (simulated value closer to 45.5 Hz). The amplitude of the voltage offset removal source is chosen such that

the SQUID voltage offset is cancelled out when the offset removal source is switched with the same frequency and phase as the bias reversal current.

5.3.1 Basic FLL Simulation

Basic Open-loop Operation

For open-loop (tuning) operation, the integrator's feedback resistor is connected in parallel with the capacitor and the FLL feedback resistor is connected to ground instead of the feedback coil.

Figure 5.3 shows the simulated outputs of the FLL for open-loop (tuning) operation with Iphi a 1 Hz triangular current corresponding to an applied flux of $1\Phi_0$. The figure shows the output of the Flux-Locked-Loop for all three calibration factors (10.2 V/Φ_0, 1.02 V/Φ_0 and 102 mV/Φ_0). The feedback resistor and integrator capacitor values are changed according to Table 5.1 above to achieve the desired calibration factors.

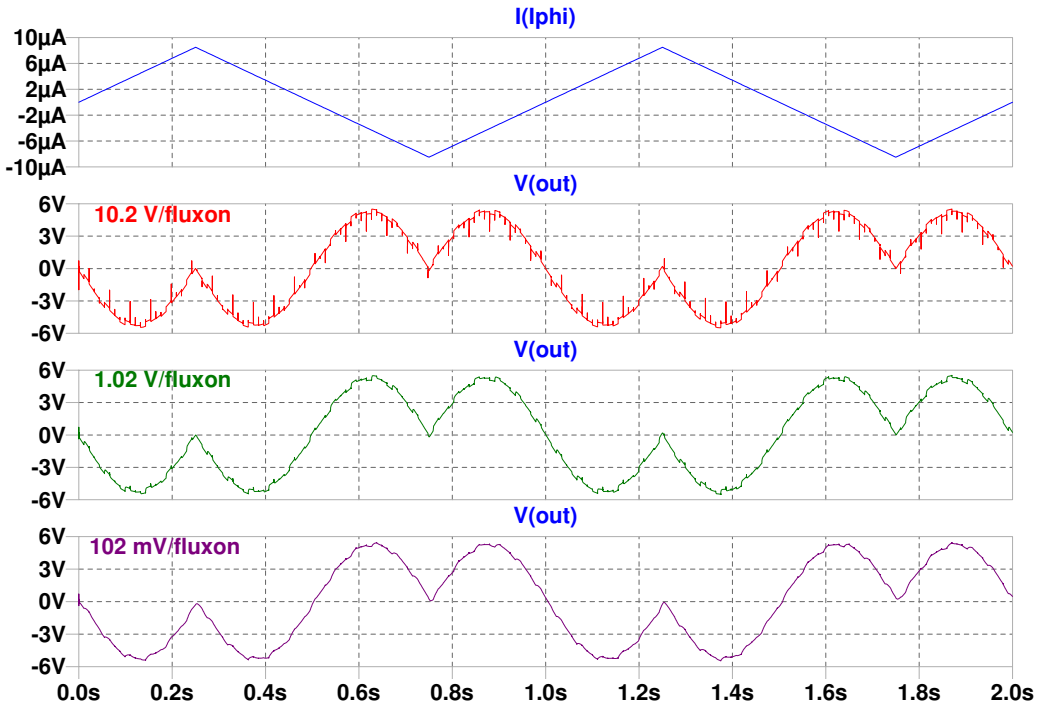


Figure 5.3: Simulated open-loop FLL results for a 1 Hz triangular test input signal with a peak-to-peak current of 17 μA corresponding to an applied magnetic flux of $1\Phi_0$. Output for all three calibration factors shown.

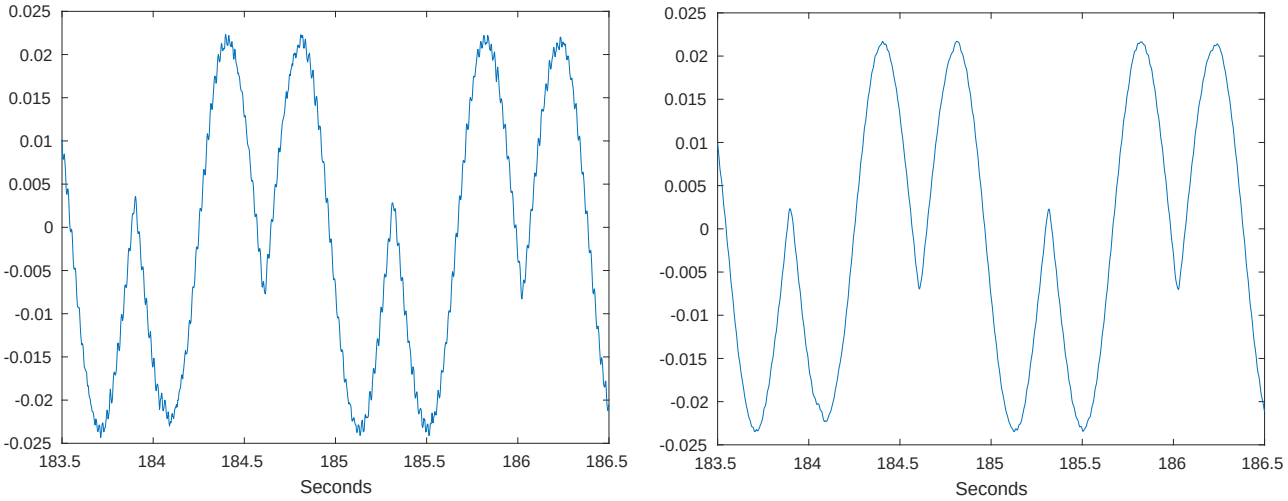
Since the integrator is designed with a gain of 1, the theoretical gain from the SQUID output to the FLL output in open-loop configuration is G = 180000. Given that the SQUID has a voltage transfer function of $\delta V/\delta\Phi_0 = 60\ \mu V/\Phi_0$, the expected peak-to-peak output voltage of the FLL is 10.8 V. The simulated peak-to-peak output voltage was approximately 10.8 V for all calibration factors, corresponding extremely well with the theoretical output.

The simulated signal appears to be quite noisy. This noise is due to a number of factors. Residual SQUID offset voltage that is not perfectly cancelled out using the offset voltage source is one cause. Small voltage offsets from the operational amplifiers prior to the lock-in detection switches is another factor. High-frequency switching transients also contribute. The noise due to the residual SQUID offset voltage could be reduced further by adjusting the voltage offset

removal signal to a more exact value. The effect of high-frequency switching transients could also be minimised with appropriate filtering after the FLL.

Figure 5.4 shows the output waveform measured from an actual SQUID at SANSA Space Science in Hermanus, South Africa using Magnicon SEL-1 control electronics. This waveform was obtained for a 0.7 Hz triangular test input signal corresponding to an applied flux of $1\Phi_0$ with the control system in open-loop configuration. Figure 5.5 shows the simulated open-loop response of the designed FLL for a 0.7 Hz triangular input corresponding to $1\Phi_0$.

The waveform obtained from the simulation results for the designed FLL corresponds extremely well with the shape of the waveform measured from an actual SQUID. This indicates that the FLL is operating exactly as desired for open-loop operation with an applied flux of $1\Phi_0$.



(a) Unfiltered output.

(b) Filtered output.

Figure 5.4: Measured open-loop waveform of an actual SQUID for a 0.7 Hz triangular test input signal corresponding to an applied magnetic flux of $1\Phi_0$ as measured at SANSA Space Science in Hermanus, South Africa using Magnicon SEL-1 control electronics. Obtained from [46] and [47].

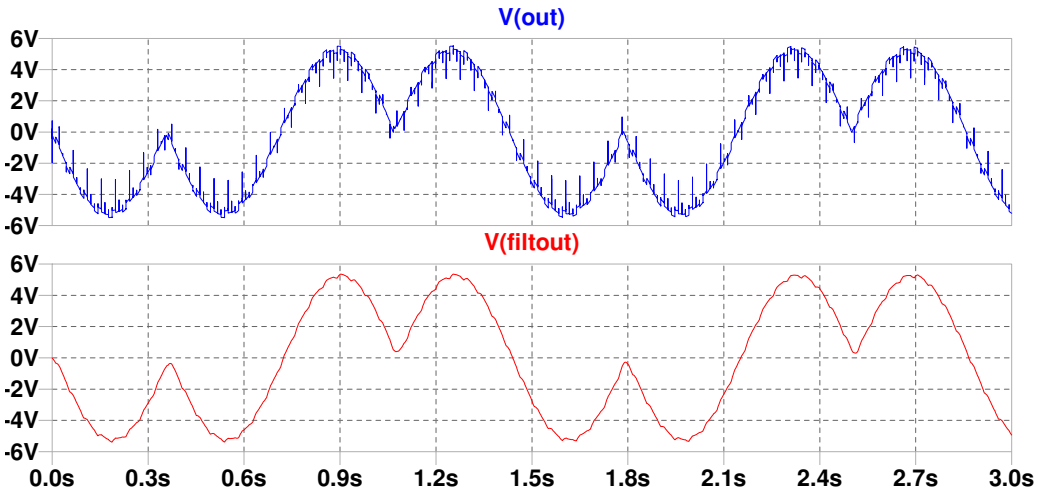


Figure 5.5: Unfiltered and filtered simulated open-loop FLL output for a 0.7 Hz triangular test input signal corresponding to an applied magnetic flux of $1\Phi_0$.

The output signal from an FLL normally undergoes additional low-pass filtering after the FLL to remove high frequency noise, smooth out the response and prevent aliasing when data is obtained using a DAQ board [3]. Figure 5.4a shows the real FLL output before processing and Figure 5.4b shows the real FLL output after digitally filtering the signal. The first plot in Figure 5.5 shows the noisy signal measured directly at the simulated FLL output. The second plot shows the same output after a simple low-pass RC filter with a cutoff frequency of approximately 16 Hz. The smooth curves in the second plot correspond very well with the expected filtered waveform from Figure 5.4.

Basic Closed-loop Operation

For closed-loop operation, the integrator's feedback resistor is disconnected and the FLL feedback resistor is connected to the feedback coil.

Figure 5.3 shows the simulated outputs of the FLL for closed-loop operation with Iphi set to a 1 Hz triangular current corresponding to an applied flux of $1\Phi_0$. The figure shows the output of the Flux-Locked-Loop for all three calibration factors (10.2 V/Φ_0, 1.02 V/Φ_0 and 102 mV/Φ_0). The feedback resistor and integrator capacitor values are changed according to Table 5.1 above to achieve the desired calibration factors.

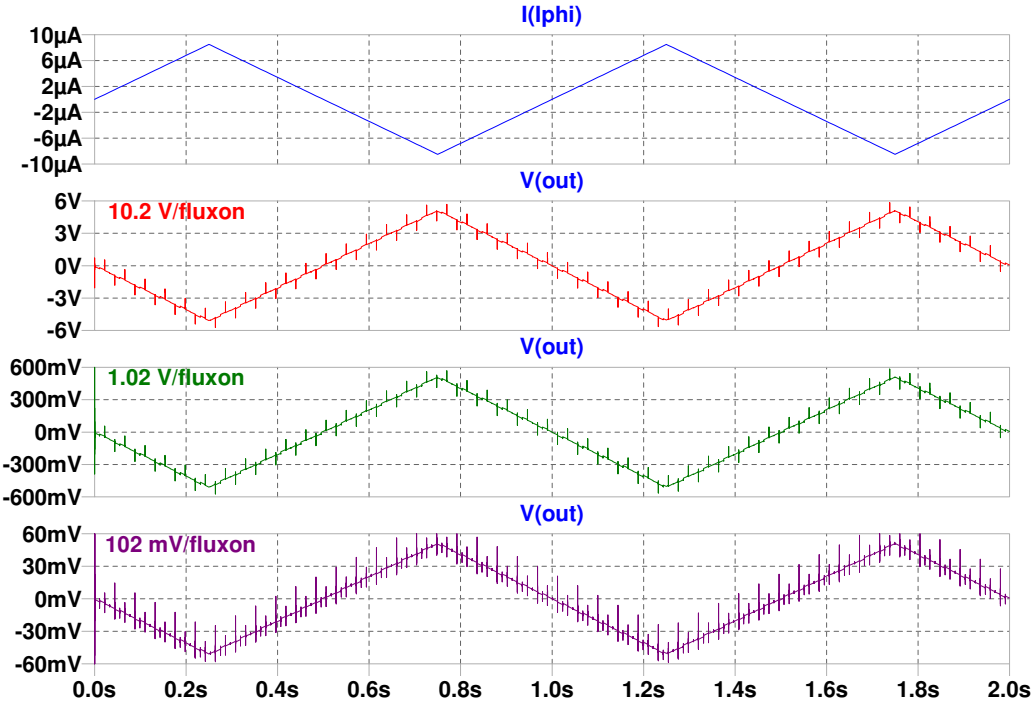


Figure 5.6: Simulated closed-loop FLL results for a 1 Hz triangular test input signal with a peak-to-peak current of 17 μA corresponding to an applied magnetic flux of $1\Phi_0$. Output for all three calibration factors shown.

The output voltage of the FLL is clearly an inverted image of the "applied flux" from the Iphi current for each of the three calibration factors. The inversion is due to the fact that the output voltage of the FLL is actually a measure of the FLL's response to remove the effect of the applied flux on the SQUID rather than a measure of the applied flux itself. A simple inverting stage after the FLL will produce an output that closely mimics the waveform shape and frequency of the applied flux.

The theoretical peak-to-peak voltage output for an applied flux of $1\Phi_0$ for each of the calibration factors is 10.2 V, 1.02 V and 102 mV. The simulated peak-to-peak output voltage corresponds extremely well with these expected values for each calibration factor.

To confirm that the FLL design was correctly tracking Iphi (and the applied flux this current represented), a sinusoidal Iphi with an amplitude of $\Phi_0/2$ and a frequency of 1 Hz was applied. Figure 5.7 shows the output of the FLL for this Iphi input. The FLL clearly tracks the sinusoidal waveform with the correct frequency and amplitude.

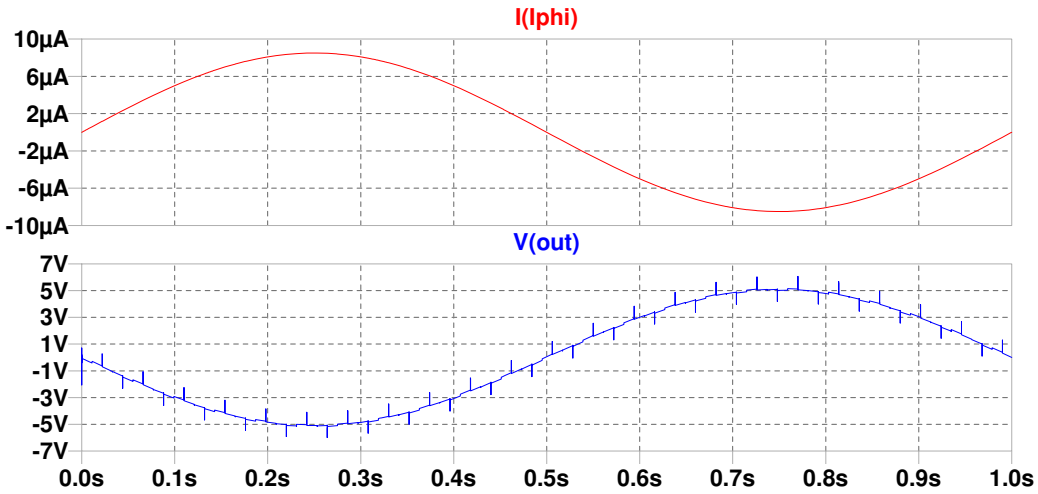


Figure 5.7: Simulated closed-loop FLL results for a 1 Hz sinusoidal test input signal with a peak-to-peak current of 17 μA corresponding to an applied magnetic flux of $1\Phi_0$. Output for a calibration factor of 10.2 V/Φ_0 shown.

Operation at Different Frequencies

The FLL was confirmed to function as desired for both open- and closed-loop operation at a frequency of 1 Hz. The next step was to check the operation of the designed FLL at higher and lower frequencies within the low frequency region of interest.

A frequency of 10 Hz was chosen to evaluate the circuit operation at slightly higher frequencies. This provides an indication of the FLL's ability to track the Earth's resonant frequency (7.83 Hz). Analysing this signal can provide useful information about thunderstorm activity in the Earth's atmosphere [48].

A frequency of 10 mHz was chosen to check the circuit operation at very low frequencies. Theoretically, the circuit should still function as desired for frequencies well below 10 mHz, but simulations take extremely long to run at these low frequencies and the data files generated are too large too effectively evaluate the FLL response. Measurements of ultra-low frequencies in the millihertz range are generally used for the detection of seismic activity [49].

Figures 5.8 and 5.9 on the next page show the response of the FLL for open-loop and closed-loop operation respectively when a 10 Hz triangular test input corresponding to $1\Phi_0$ is applied. The calibration factor was set to 10.2 V/Φ_0. The testing of different calibration factors is discussed in the next section.

Both the open-loop and closed-loop response of the simulated FLL closely matched the expected results for a frequency of 10 Hz. The peak-to-peak voltage outputs are close to 10.8 V for open-loop operation and 10.2 V for closed-loop operation as desired.

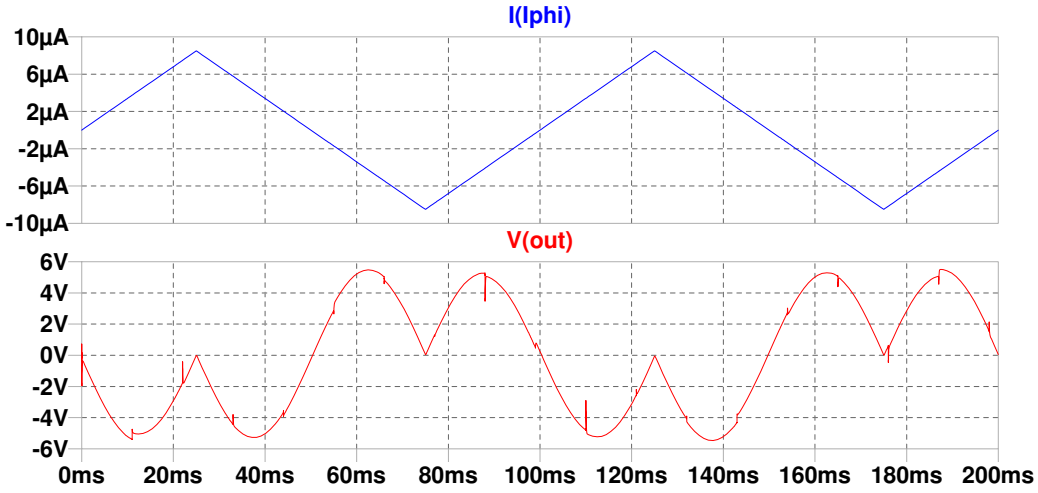


Figure 5.8: Simulated open-loop FLL results for a 10 Hz triangular test input signal corresponding to an applied magnetic flux of $1\Phi_0$. Output for a calibration factor of 10.2 V/Φ_0 shown.

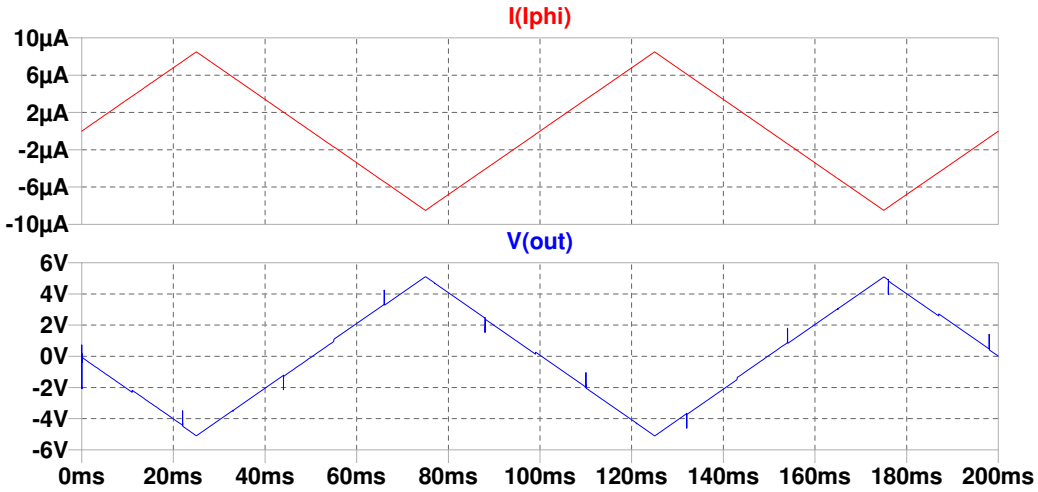


Figure 5.9: Simulated closed-loop FLL results for a 10 Hz triangular test input signal corresponding to an applied magnetic flux of $1\Phi_0$. Output for a calibration factor of 10.2 V/Φ_0 shown.

Figures 5.10 and 5.11 on the next page show the response of the FLL to a 10 mHz triangular test input corresponding to $1\Phi_0$ with a calibration factor of 10.2 V/Φ_0 for open-loop and closed-loop operation respectively. The first plot in each figure shows the applied Iphi signal. The second shows the voltage measured directly at the output of the FLL.

For the 10 mHz outputs, the high frequency noise discussed earlier has more of an impact on the output of the FLL. While the desired waveform shape is clearly visible, the peak-to-peak voltage is harder to determine due to this noise. If a RC low-pass filter with a cutoff frequency of approximately 50 Hz is used at the output of the FLL, the noise is attenuated and the output voltage is much clearer. The third plot for each of the figures shows the output after the filter.

This provides a clear indication that low frequency measurements can be successfully made using the designed FLL if appropriate filtering is included at the output. Having a range of

available filters at the output would be useful since the user could select the most suitable filter for the signal of interest.

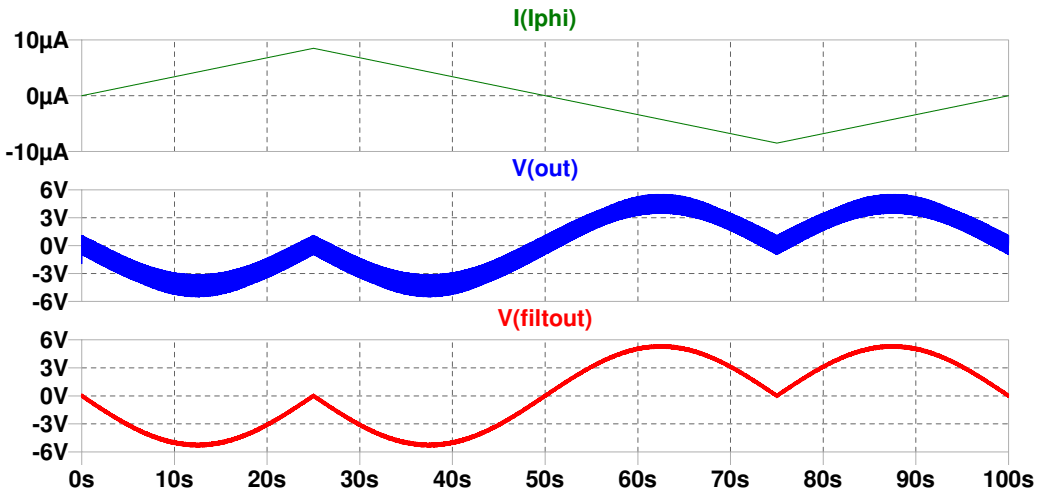


Figure 5.10: Simulated open-loop FLL results for a 10 mHz triangular test input signal corresponding to an applied magnetic flux of $1\Phi_0$. Output for a calibration factor of 10.2 V/Φ_0 shown.

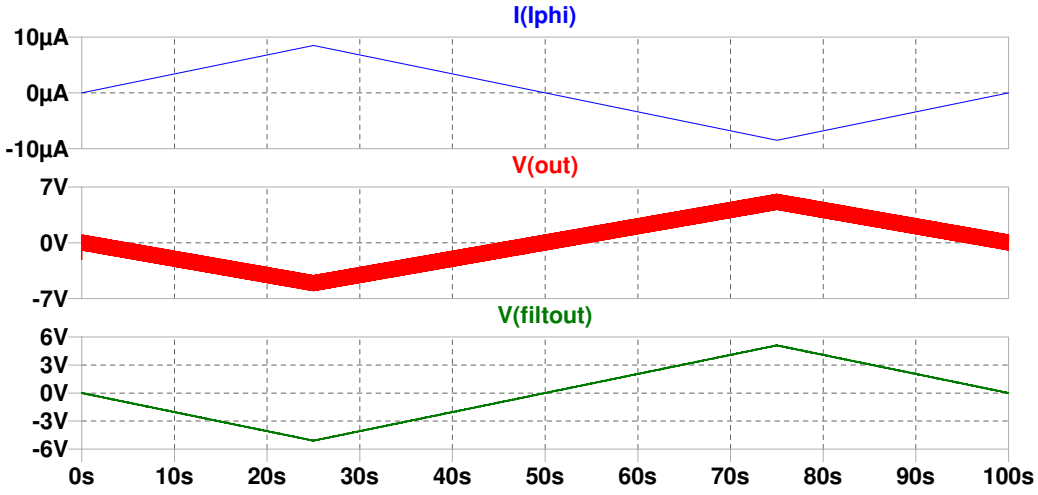


Figure 5.11: Simulated closed-loop FLL results for a 10 mHz triangular test input signal corresponding to an applied magnetic flux of $1\Phi_0$. Output for a calibration factor of 10.2 V/Φ_0 shown.

Fluxon Range Results

Since the FLL was confirmed to function as desired for both open-loop and closed-loop operation at a range of frequencies, the next step was to check the closed-loop response for a range of Φ_0 values.

According to Table 5.1, the maximum measurable Φ_0 value is $196\Phi_0$ using a calibration factor of 102 mV/Φ_0 and assuming a voltage range of ± 10 V. From 2.1, the field calibration of the M2700 is known to be 33 nT/Φ_0. Therefore, an applied flux of $196\Phi_0$ corresponds to a maximum measurable magnetic field range of 6.468 μT (which is well outside the typical quiet daily variation of about 100 nT in Earth's magnetic field).

When the FLL was simulated with a test input corresponding to $196\Phi_0$, the signal clipped at the voltage rails. This is due to the fact that the integrator operational amplifier saturates at a voltage slightly lower than 10 V. Figure 5.12 shows the FLL closed-loop output for a 1 Hz triangular test input signal corresponding to an applied magnetic flux of $195\Phi_0$ for a calibration factor of 102 mV/ϕ_0. The output of the FLL correctly tracks the input Iphi with the expected peak-to-peak voltage. This indicates that the FLL can successfully measure a maximum magnetic field range of 6.435 μT.

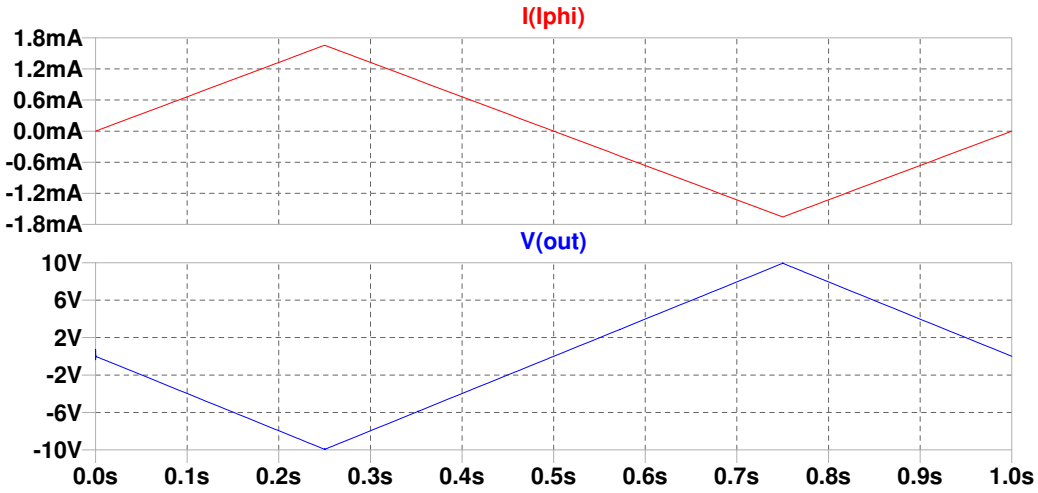


Figure 5.12: Simulated closed-loop FLL results for a 1 Hz triangular test input signal corresponding to an applied magnetic flux of $195\Phi_0$. Output for a calibration factor of 102 mV/Φ_0 shown.

It was also necessary to determine the smallest range of Φ_0 values that the FLL can successfully track. Figure 5.13 shows the simulated closed-loop FLL output for a 1 Hz triangular test input corresponding to an applied magnetic flux of $0.005\Phi_0$ at a calibration factor of 10.2 V/Φ_0.

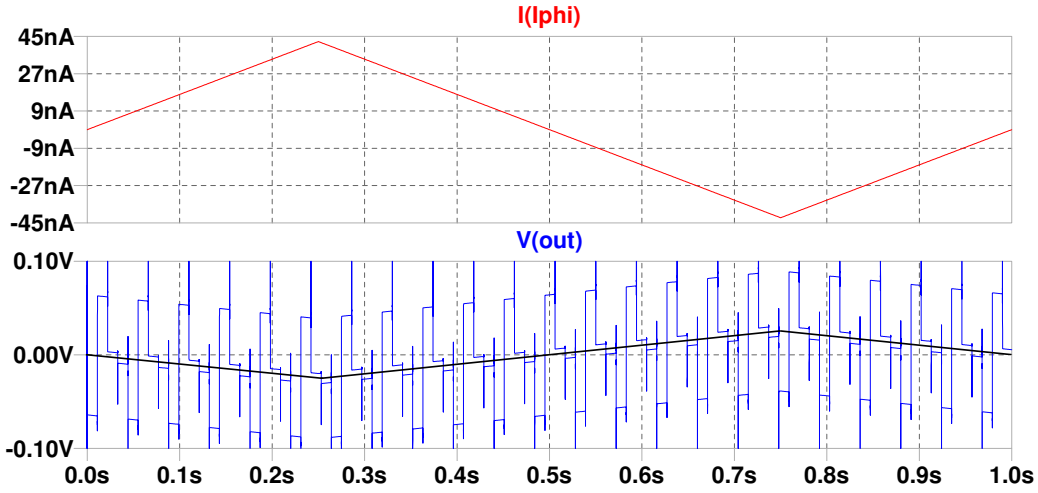


Figure 5.13: Simulated closed-loop FLL results for a 1 Hz triangular test input signal corresponding to an applied magnetic flux of $0.005\Phi_0$. Output for a calibration factor of 10.2 V/Φ_0 shown.

The magnetic field range corresponding to an applied flux of $0.005\Phi_0$ is 0.165 nT. At this extremely low value, the residual SQUID offset voltage and small voltage offsets of the operational

amplifier have a very noticeable effect on the output of the FLL, partially hiding the desired signal. The black line drawn through the centre of the simulated response shows the desired signal hidden in the noise.

The first plot in Figure 5.14 shows the simulated output of the FLL when the value of the voltage source used to remove the SQUID offset is adjusted for a more accurate result. The switching output after this is due to the small voltage offsets of the operational amplifiers and is less easily reduced. The second plot shows the same output after a simple low-pass RC filter with a very lot cutoff of 2.7 Hz. The amplitude of the output voltage is expected to be 25.5 mV for $0.005\Phi_0$ and the filtered response is a little under 25 mV. The filtered output almost tracks the Iphi value as desired but there is a significant delay of approximately 50 ms due to the low-pass filter.

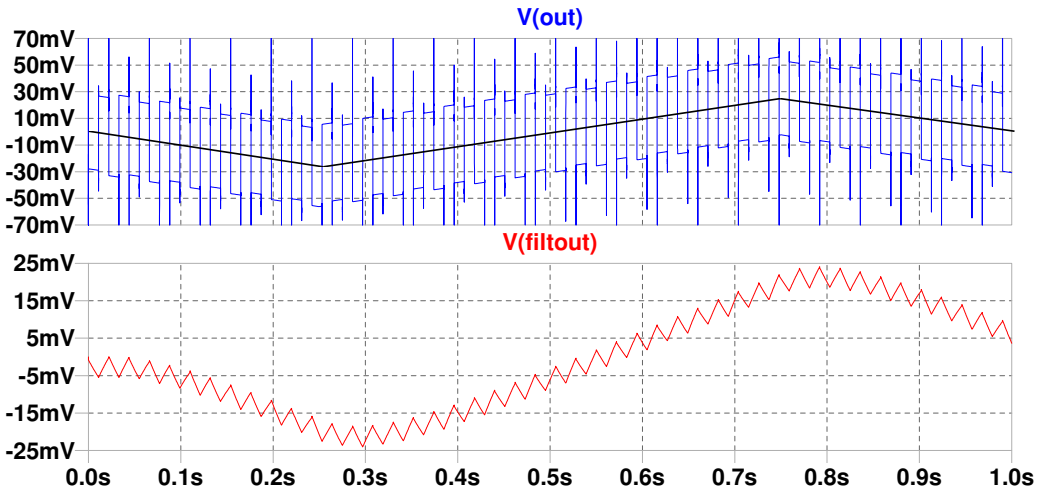


Figure 5.14: Simulated closed-loop FLL output for a 1 Hz triangular test input signal corresponding to an applied magnetic flux of $0.005\Phi_0$. Output for a calibration factor of 10.2 V/Φ_0 with improved voltage offset removal.

5.3.2 FLL Simulation including Noise

The simulated FLL appears to function correctly for a wide range of applied magnetic fields and frequencies. The simulations implemented so far, however, had not considered the effect of the pre-amplifier noise on the voltage output.

From Section 4.4, the flatband equivalent input noise of the pre-amplifier at the SQUID was calculated as 0.190 $nV/\sqrt{Hz}$ with a corner frequency of approximately 6 mHz. This correspond to a flux noise of approximately 3 $\mu\Phi_0/\sqrt{Hz}$. The noise of the M2700 was given as being 300 $fT/\sqrt{Hz}$ for frequencies down to 10 Hz. This corresponds to a noise flux of 9 $\mu\Phi_0/\sqrt{Hz}$. This means that the noise of the SQUID itself is considerably larger than the noise contributed by the pre-amplifier.

According to [50], the peak-to-peak voltage noise of a circuit can be determined by multiplying the RMS noise by 6.6. The RMS noise contribution of the pre-amplifier was determined to be 13.486 V_{RMS} earlier. The peak-to-peak noise voltage contribution of the pre-amplifier is therefore $V_{noise} = 94.384$ nV.

The FLL can then be simulated including the effect of the peak-to-peak voltage noise of the pre-amplifier. This can be implemented in LTspice using a white noise voltage source with a

peak-to-peak value equal to 94.384 nV and a frequency determined by multiplying the closed-loop bandwidth of the system by the time step used for transient simulation. The white noise voltage source is added to the output of the modelled SQUID before the transformer.

Figures 5.15 and 5.16 show the output of the FLL including pre-amplifier noise for a 1 Hz triangular test input corresponding with an applied flux of $1\Phi_0$ for open-loop and closed-loop operation respectively. The calibration factor was set to 10.2 V/Φ_0. In both cases, the second plot is simply a zoomed-in cross section of the first plot. The blue curve is the output without added noise while the red curve includes the effect of the pre-amplifier noise.

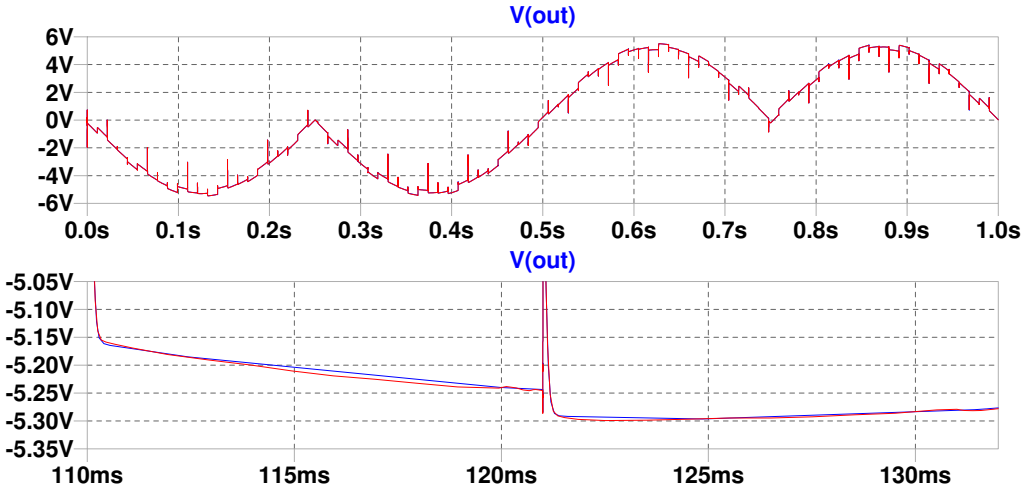


Figure 5.15: Simulated open-loop FLL output including pre-amplifier noise for a 1 Hz triangular test input signal corresponding to an applied magnetic flux of $1\Phi_0$. Calibration factor is set to 10.2 V/Φ_0.

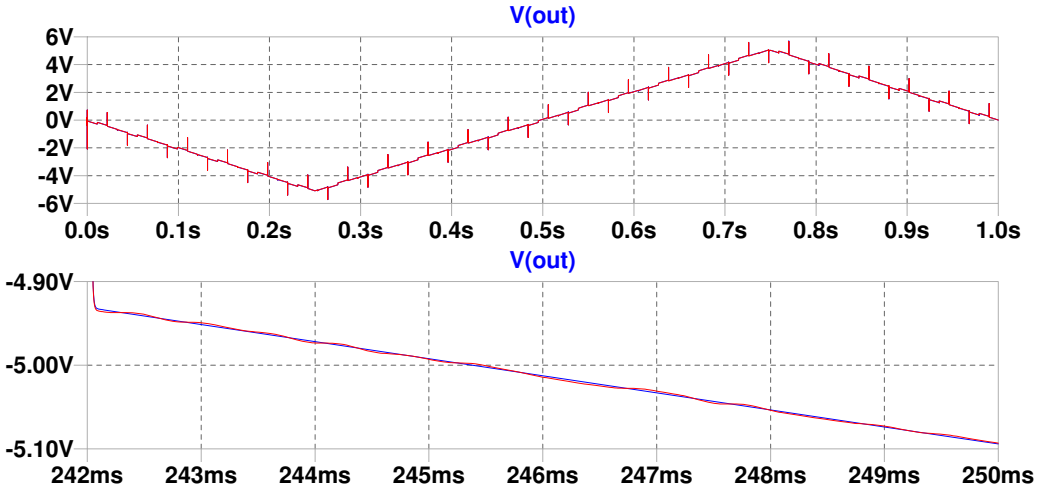


Figure 5.16: Simulated closed-loop FLL output including pre-amplifier noise for a 1 Hz triangular test input signal corresponding to an applied magnetic flux of $1\Phi_0$. Calibration factor is set to 10.2 V/Φ_0.

For both open-loop and closed-loop operation, the effect of the added pre-amplifier noise on the voltage output is almost negligible and, especially in the closed-loop case, hardly distinguishable from the case without added noise.

While the noise response for an applied flux of $1\Phi_0$ is very good, the response needs to be evaluated for the low end of the measurable Φ_0 range. Figure 5.17 shows the closed-loop output voltage of the FLL for an applied flux of $0.005\Phi_0$ when the offset voltage removal source has been tuned to the best possible response. Figure 5.18 shows the same output after the 2.7 Hz low-pass filter was applied, as discussed earlier. In both cases, the first plot shows the output without added noise and the second plot shows the output including the effect of pre-amplifier noise.

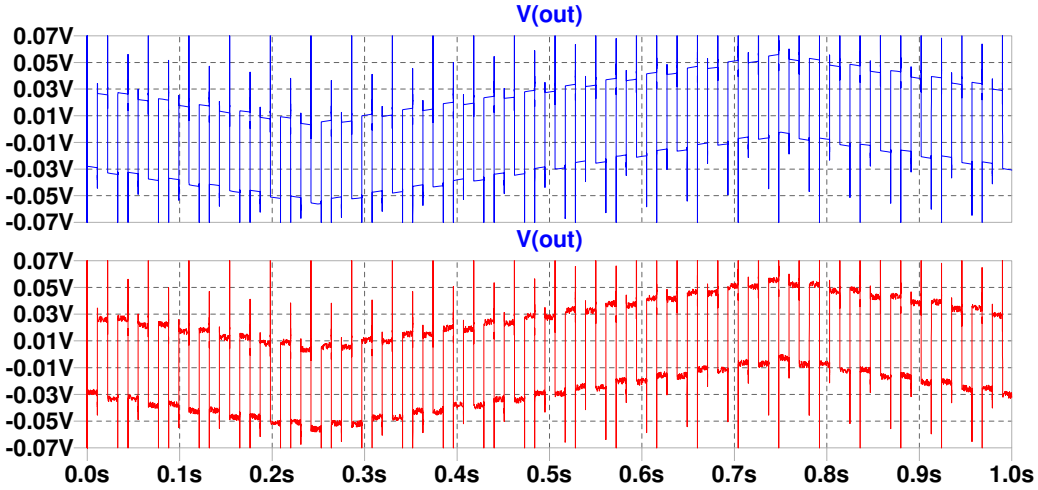


Figure 5.17: Simulated closed-loop FLL output including pre-amplifier noise for a 1 Hz triangular test input signal corresponding to an applied magnetic flux of $0.005\Phi_0$. Calibration factor is set to 10.2 V/Φ_0.

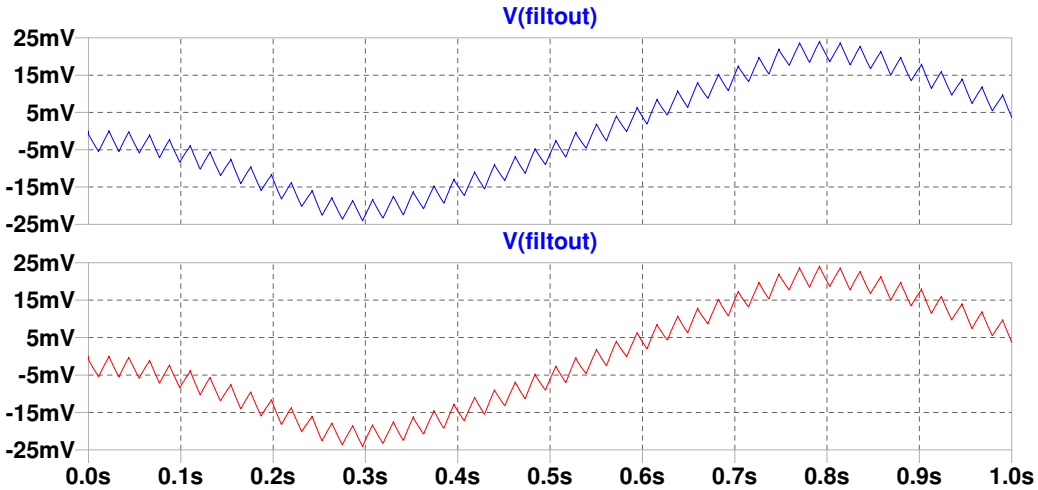


Figure 5.18: Filtered simulated closed-loop FLL output including pre-amplifier noise for a 1 Hz triangular test input signal corresponding to an applied magnetic flux of $0.005\Phi_0$. Calibration factor is set to 10.2 V/Φ_0.

For this small magnetic field measurement, the pre-amplifier noise has a much larger impact on the simulated output signal. After filtering, however, the outputs with and without noise are practically identical.

Full analysis

Since the simulated FLL appears to respond desirably to different frequencies, magnetic field magnitudes and the addition of pre-amplifier noise for both open-loop and closed-loop operation, a final simulation was performed that implemented a combination of these factors for a worst case scenario measurement.

Figure 5.19 shows the simulated closed-loop output of the FLL for a 10 mHz sinusoidal Iphi corresponding to a magnetic flux of $0.005\Phi_0$ with noise from the pre-amplifier included. The calibration factor was set to 10.2 V/Φ_0. The second plot shows the output without any filtering. The third and fourth plots show the output after a 2.7 Hz low-pass RC filter where the third plot does not include the pre-amplifier noise contribution and the fourth plot does.

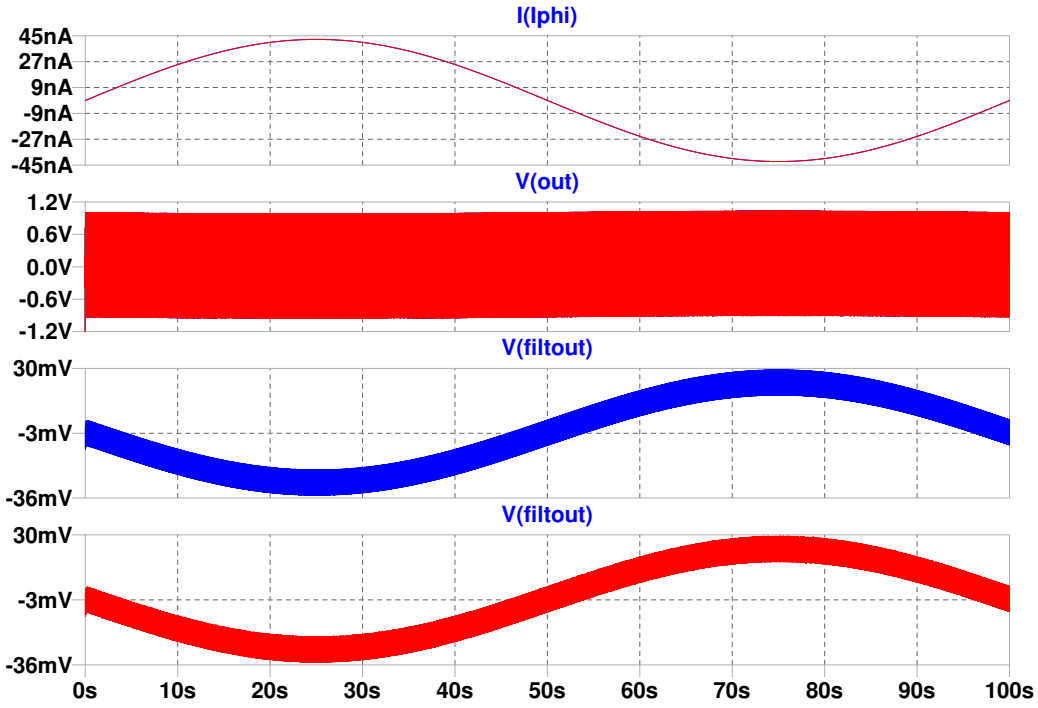


Figure 5.19: Simulated closed-loop FLL results including pre-amplifier noise for a 10 mHz sinusoidal test input signal corresponding to an applied magnetic flux of $0.005\Phi_0$. Calibration factor is set to 10.2 V/Φ_0.

Measuring the simulated output directly from the FLL produced a signal with no resemblance to the sinusoidal Iphi representing the $0.005\Phi_0$ applied flux. The simulated output after the 2.7 Hz low-pass filter, however, appeared to closely track the sinusoidal waveform.

It is very difficult to determine from the third and fourth plot what effect the added pre-amplifier noise has on the output of the FLL. To better evaluate this, a zoomed-in cross section of the outputs in Figure 5.19 is shown in Figure 5.20 on the next page.

The output of the FLL without any filtering is shown in the first plot. The blue signal represents the system without added noise and the red signal includes pre-amplifier noise. The second plot shows the filtered output without added noise and the third plot shows the filtered output including pre-amplifier noise.

The effect of the pre-amplifier noise is visible as a jitter in the output of the FLL on the first plot, but this noise does not in any way mask the actual measurement. This indicates that it

has minimal effect on the sensitivity of the SQUID. The filtered outputs in the second and third plots are almost identical, so the effect of the pre-amplifier noise at this low magnetic field level can be considered to be negligible.

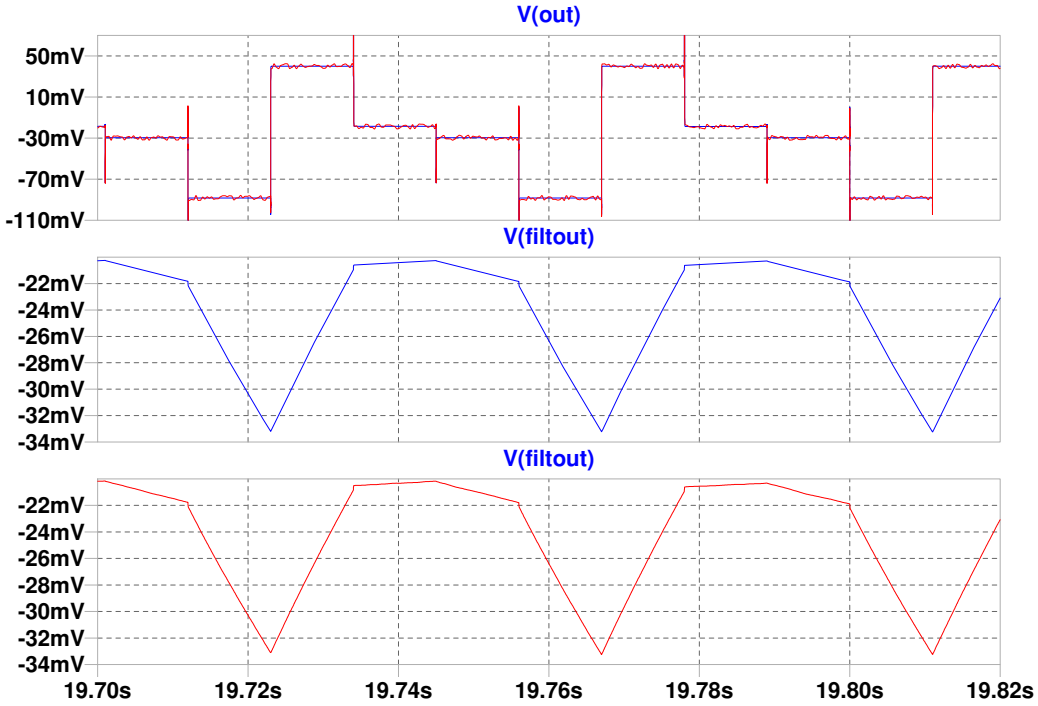


Figure 5.20: Cross-section of the simulated closed-loop FLL output including pre-amplifier noise for a 10 mHz sinusoidal test input signal corresponding to an applied magnetic flux of $0.005\Phi_0$. Calibration factor is set to 10.2 mV/Φ_0.

The results obtained from these simulations provide a clear indication that the FLL design considered in this research could be implemented for use on an actual SQUID measuring low frequency signals.

Chapter 6

Conclusion and Recommendations

6.1 Review of Project Objectives

A review of the objectives in Section 1.3 provides a good indication of the success of the proposed Flux-Locked-Loop design and whether the desired requirements are met.

Objective 1 - The proposed design should accurately track magnetic fields with ultra-low frequencies

The selected pre-amplifier design in Chapter 4 utilises DC coupling to avoid the low cutoff frequencies caused by capacitors. This theoretically allows the FLL to measure frequencies all the way down to the DC level. The proposed full FLL design was simulated for an input with a low frequency of 10 mHz in Chapter 5. With appropriate low-pass filtering of the output signal, the desired response was obtained. Simulations were not implemented at lower frequencies due to the excessively long simulation times, but it is assumed that the design will still function as desired for frequencies of 1 mHz and lower with appropriate filtering.

Objective 2 - The proposed design should measure a large range of magnetic flux densities

The FLL was designed for three potential calibration factors: 10.2 V/Φ_0, 1.02 V/Φ_0 and 102 mV/Φ_0. These calibration factors allowed for the selection of three different measurement ranges for high, medium and low sensitivity.

The maximum measurable flux change was obtained by simulation using the low sensitivity setting of 102 mV/Φ_0. The maximum magnetic flux that was simulated successfully was $195\Phi_0$. The minimum measurable flux change was not explicitly determined, but using the high sensitivity setting of 10.2V/Φ_0, a magnetic flux input of $0.005\Phi_0$ was simulated. The desired response could be obtained if additional low-pass filtering was used at the output of the simulated FLL.

Therefore, the measurable magnetic flux range of the FLL determined by simulation is from $0.005\Phi_0$ to $195\Phi_0$. For the M2700 magnetometer, these magnetic flux values correspond to magnetic field magnitudes of 0.165 nT to 6.435 μT.

Objective 3 - The proposed design should be customisable for SQUIDs with different specifications

The microcontroller discussed in Chapter 3 would be used to adjust the following:

- The amplitude of the flux modulation current
- The amplitude of the bias reversal current
- The amplitude of the flux offset current
- The amplitude of the voltage offset removal signal
- The base frequency (chosen as approximately 45 Hz in this thesis)

The FLL was designed for three calibration factors using different feedback resistors and integrator capacitors. The appropriate components for the desired SQUID and measurements would be selected using the microcontroller.

Objective 4 - The proposed design should allow for both open-loop and closed-loop operation

The proposed FLL design includes a SPST switch to connect and disconnect the integrator feedback resistor for open-loop and closed-loop operation respectively. Additionally, a SPDT switch is included between the feedback resistor and feedback coil that can connect the resistor to ground for open-loop operation and to the feedback coil for closed-loop operation. These switches would be controlled from the system's microcontroller.

Objective 5 - The proposed design should contribute minimal noise to the SQUID measurements

The selected pre-amplifier from Chapter 4 was designed for extremely low noise operation. With the optional transformer from the M2700 package included, the noise contribution of the pre-amplifier at the SQUID was determined to be even lower than the noise of the SQUID itself.

The voltage noise density of the DAC8812 DACS used to provide the bias current, flux modulation current, flux offset and voltage offset removal was specified as being quite low in the flatband region. However, the effect of the noise of the DACs at the output of the SQUID was not considered in this research.

Objective 6 - The proposed design should implement flux modulation and bias current reversal to improve the noise performance of the SQUID

Chapter 3 contains a detailed description of the proposed method for implementing flux modulation, bias current reversal and lock-in detection.

Objective 7 - The proposed design should be possible to implement using readily available low-cost electronic components

All components for the proposed FLL design are readily available from electronics suppliers. No specialised high-cost components would be required to implement the design.

6.2 Challenges and Potential Improvements

As seen from the full FLL simulations in Chapter 5, the voltage offset of the operational amplifiers before the lock-in detection SPST switches can cause a square wave signal to be visible over the output of the FLL. The effect of this square wave is minimal for larger flux measurements (relative to the calibration factor) and can be smoothed away with appropriate filtering. For small flux measurements ($0.005\Phi_0$ with calibration factor of 10.2 V/Φ_0) however, the desired response is partially masked by the square wave.

To minimise this effect, different operational amplifiers could be chosen for the secondary amplification stage and the inverter from the lock-in detection stage. These operational amplifiers could be chosen with the focus on extremely low voltage offsets as opposed to low noise performance. Alternatively, additional compensation voltages could be provided at each operational amplifier to counteract the effects of the voltage offset.

One issue not considered in this thesis is the effect of potential phase shifts between the feedback coil and input to the pre-amplifier. Any phase shift at this stage would cause a problem at the lock-in detection stage, since the signal used for lock-in detection is based on the phase of the bias current and flux modulation signals before any potential phase shifts. If the phase of the signal at the output of the amplification stages is not as expected, the FLL won't correctly lock onto the desired signal.

This could be fixed by introducing an adjustable phase-shifter at the point that the reference signal is supplied to the lock-in detector. This phase-shifter could be controlled from the microcontroller so that the FLL can accurately lock onto the desired signal.

6.3 Recommendations for Future Work

Control Software and User Interface

The software used to control the FLL via a microcontroller would need to be developed including all required functionality for adjusting the output of the DACs in the system. The calibration curves of the DACs would need to be determined so that their output would accurately correspond with the value selected in the software. A simple and easy-to-use user interface would also need to be designed.

Filtering of FLL Output

From the simulations in Chapter 5, it was evident that filtering of the FLL output would be required to produce clean output responses, especially for extremely low frequency measurements. Some of this filtering could be implemented using software, once the output has been digitised using a Data Acquisition (DAQ) system. Having a range of selectable low-pass analog filters with appropriate cutoff frequencies at the output of the FLL would also be desirable. Fourth-order Butterworth filters would be suitable for this application due to their flat response in the passband and sharp cutoff.

Noise Analysis of the full FLL

A detailed noise analysis of the pre-amplifier was presented in this thesis, but the noise contributions of the other sections of the FLL were not considered. A full noise analysis would

have to be implemented that considers the flux noise contributions of the integrator and DACs at the feedback stage. Additionally, the effect of the noise of the DAC used to supply bias current to the SQUID would need to be carefully considered, since this noise is added directly to the SQUID.

PCB Design, Manufacture and Testing

Once the control software has been developed, the FLL fully analysed and necessary circuit improvements made, a PCB should be designed that includes all required components of the FLL in a compact design with appropriate isolation and shielding between analog and digital signals. Thereafter, the FLL could be manufactured and tested on an actual SQUID, possibly at SANSA in Hermanus.

6.4 Conclusion

The work presented in this thesis includes a viable design of a Flux-Locked-Loop control system including flux modulation and bias current reversal. It meets the project objectives detailed above and constitutes a promising step forward in reaching the goal of creating accessible low-cost SQUID readout electronics for low frequency magnetic field measurements.

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Appendix A

Conference Presentation Abstract - Simulation Model For a Low Cost HTS Squid System

This appendix contains the abstract that was published in the proceedings of the Student Conference on Sensors, Systems and Measurement. The abstract serves as a summary of the work presented during this online conference hosted by the Czech Technical University in Prague in June 2021.

SIMULATION MODEL FOR A LOW COST HTS SQUID SYSTEM

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1. INTRODUCTION

Commercial high temperature superconductor (HTS) superconducting quantum interference device (SQUID) systems, which are used as extremely sensitive magnetometers, are prohibitively expensive if multiple SQUID measurement stations are planned. The HTS SQUID sensors are expensive due to thin-film fabrication requirements, and the control electronics are rendered expensive due to very low production volumes. HTS SQUID sensors are not off-the-shelf items, could have a manufacturing lead time of a year, and are extremely expensive due to the manufacturing process. In addition to sourcing a low-cost HTS SQUID device, it is important to design a custom FLL and control electronics.

2. METHODS AND RESULTS

2.1 SQUID magnetometer

A first step in this process is the simulation of a SQUID magnetometer to test the flux-locked-loop (FLL) and electronics design. To use the SQUID as a magnetometer for low frequency applications, a control system known as a flux-locked loop is required to linearize the SQUID transfer function while keeping added noise to a minimum. In a flux-locked loop, the SQUID voltage is amplified, lock-in detected, integrated, and fed back to the SQUID as a current through a feedback coil. The combination of flux modulation and bias current reversal in this control system ensures that the SQUID is biased at the points of lowest noise and that the 1/f noise due to critical current fluctuations is suppressed.

2.2 SPICE simulation of the full (FLL) SQUID system

The proposed design includes a low noise amplifier consisting of a bipolar input stage with a gain larger than one hundred and secondary amplification stages using low noise high precision operational amplifiers. The high gain of the input stage ensures that the noise produced in the subsequent amplification stages is essentially negligible. Lock in detection is achieved using synchronous switches with the product of the modulation and bias frequencies used as a reference signal. Both the integrator and secondary amplification stages are designed for flexibility to cater for different SQUID output ranges and allow for adjustments in the system's sensitivity.

The FLL system (SQUID bias, amplification and demodulation) has been simulated in LTspice with a dependent voltage source used to simulate a SQUID response to flux input – Fig. 1. The initial results have been very promising, with the V-Phi characteristics shown by the open-loop output of the flux-locked loop closely resembling the real V-Phi characteristics measured from an actual SQUID for a triangular flux input -- see Fig. 2. In addition, the simulated closed-loop output closely resembled the applied input flux waveform and the equivalent input noise of the FLL is quite low (in the region of 1 nV/√Hz). The end goal is to

produce dedicated low frequency SQUID readout electronics that are easy to control and implement. At this time only the design of the control electronics is considered, a commercial data acquisition unit will be used for data acquisition.

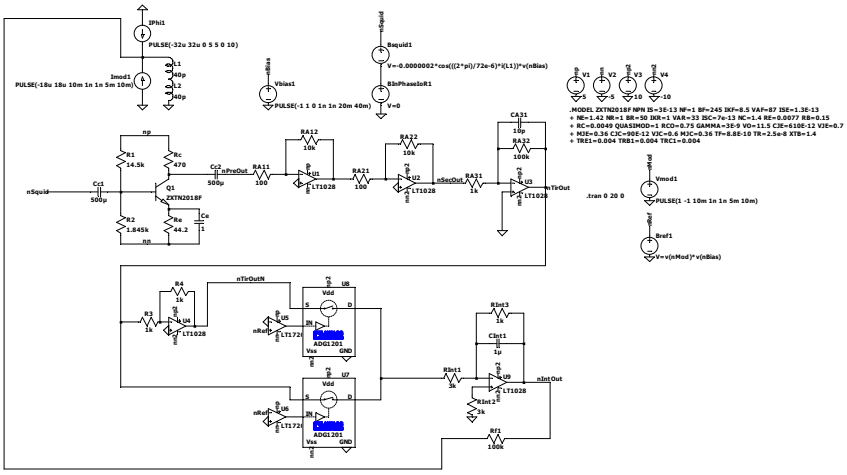

Figure 1. LTspice schematic of the flux-locked loop design

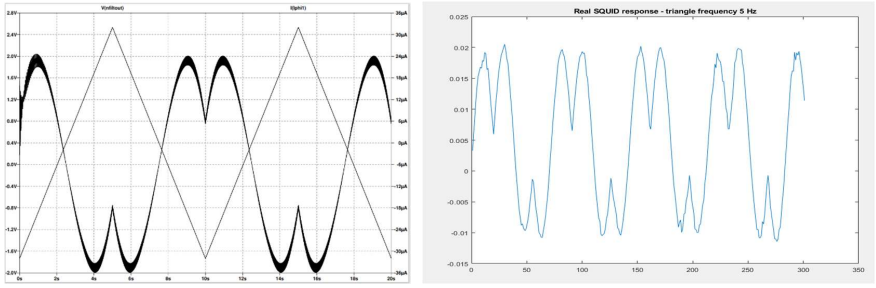

Figure 2. Simulated open-loop response at 100 mHz (left) and the real open-loop response of a M2700 SQUID measured unshielded at SANSA Hermanus (right)

3. CONCLUSION

The initial simulation results are promising with both the open and closed-loop waveforms resembling the expected output of a real SQUID. Transient simulations including noise produced in the FLL could provide better insight into the suitability of the design.

ACKNOWLEDGMENT

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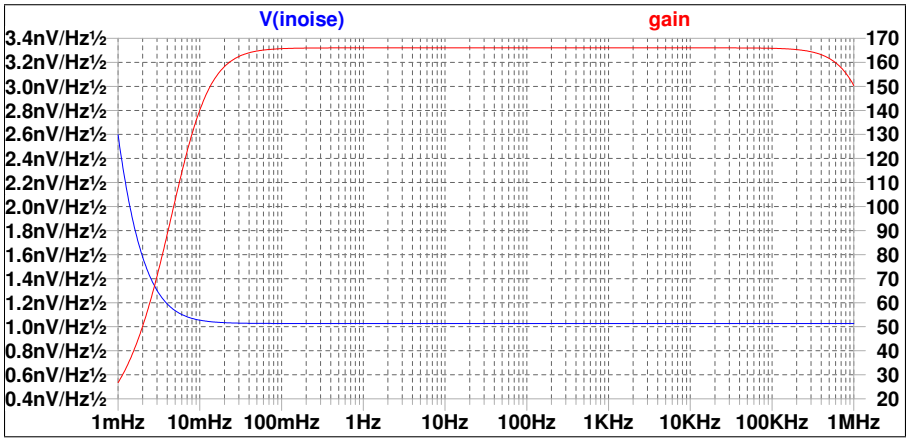
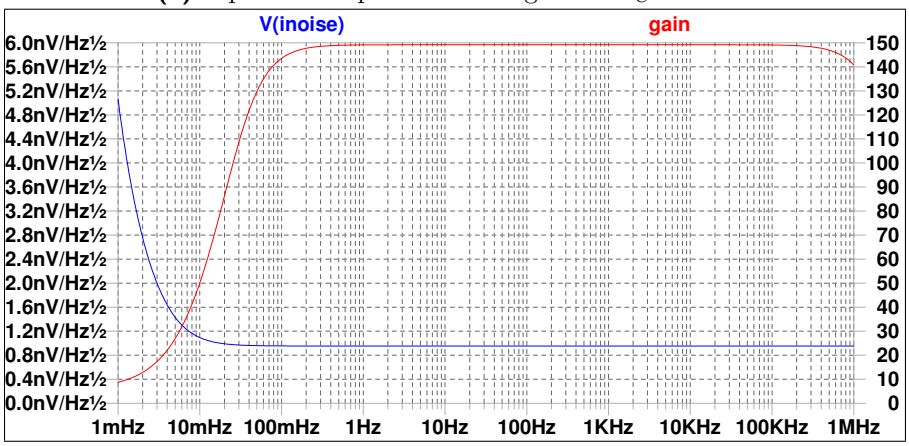
Appendix B

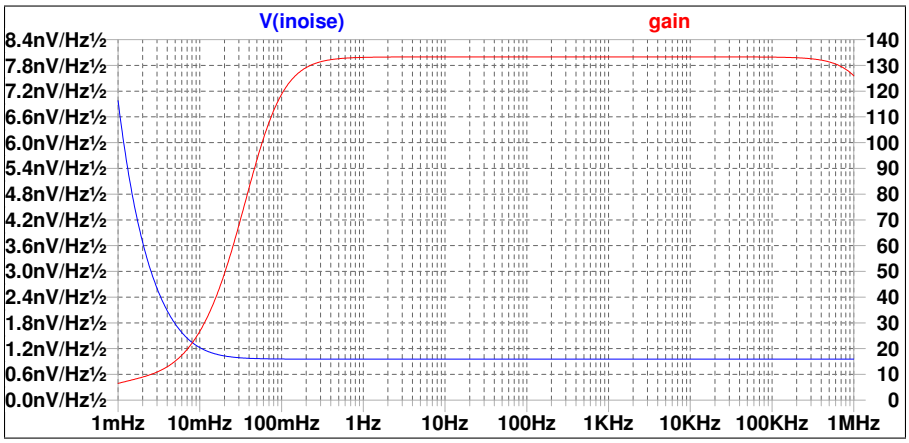
Common Emitter Amplifier Simulation Results



(a) Equivalent input noise and gain for $I_C = 1$ mA

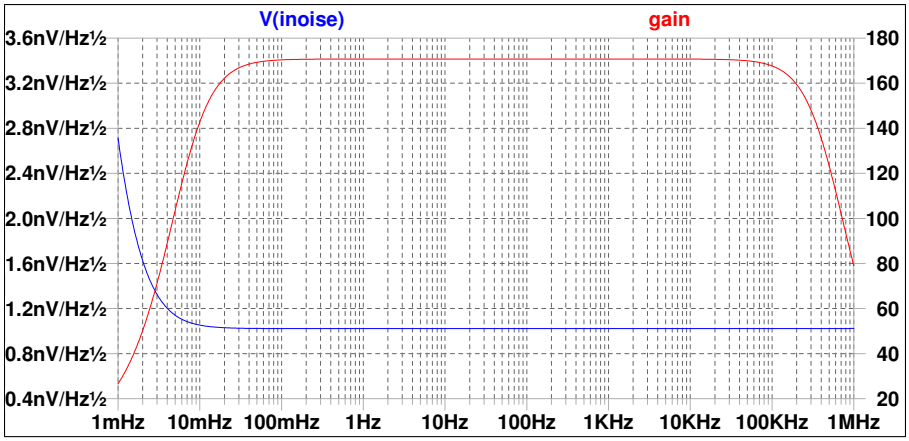


(b) Equivalent input noise and gain for $I_C = 5$ mA

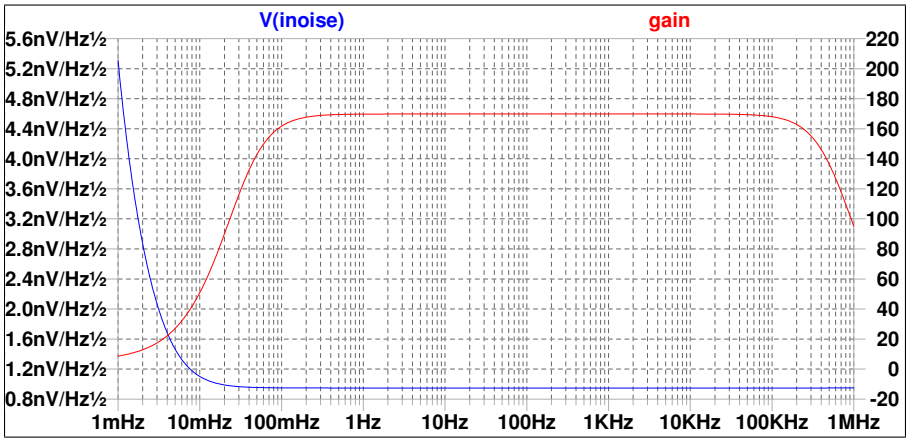


(c) Equivalent input noise and gain for $I_C = 10$ mA

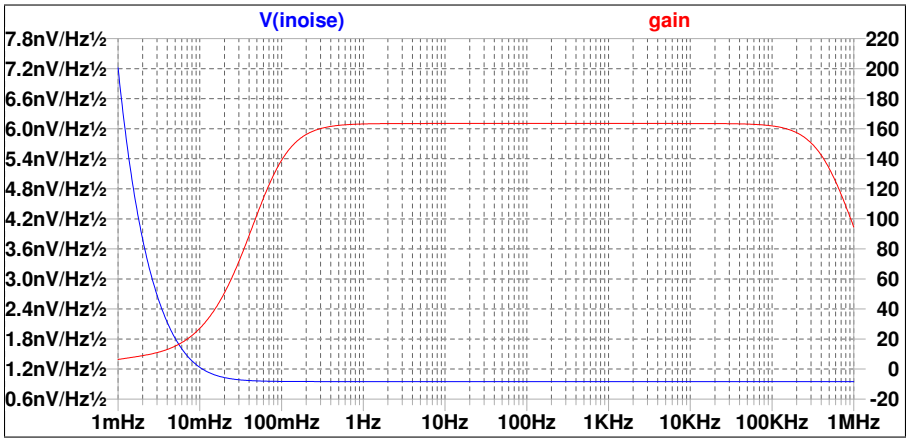
Figure B.1: Simulation results of 2SA1312 transistor.



(a) Equivalent input noise and gain for $I_C = 1$ mA

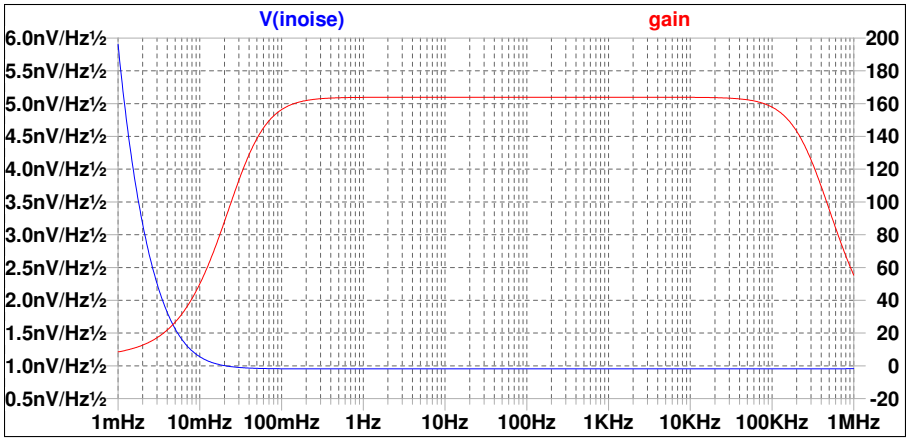


(b) Equivalent input noise and gain for $I_C = 5$ mA

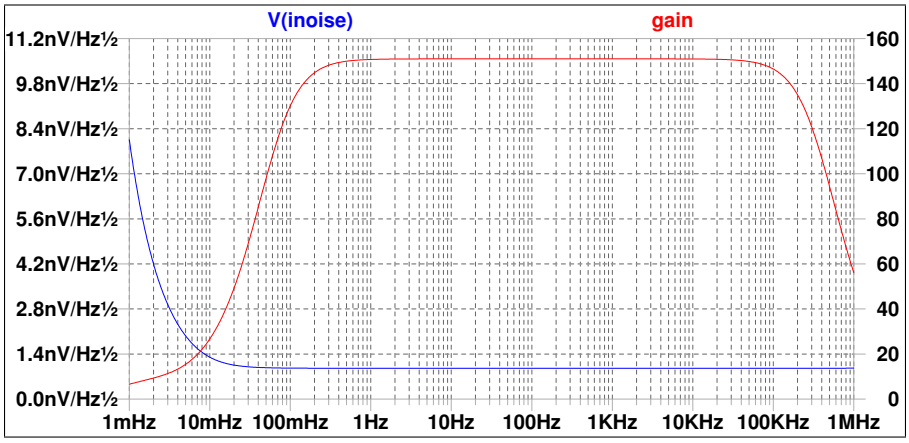


(c) Equivalent input noise and gain for $I_C = 10$ mA

Figure B.2: Simulation results of DSS20201L transistor.



(a) Equivalent input noise and gain for $I_C = 5$ mA

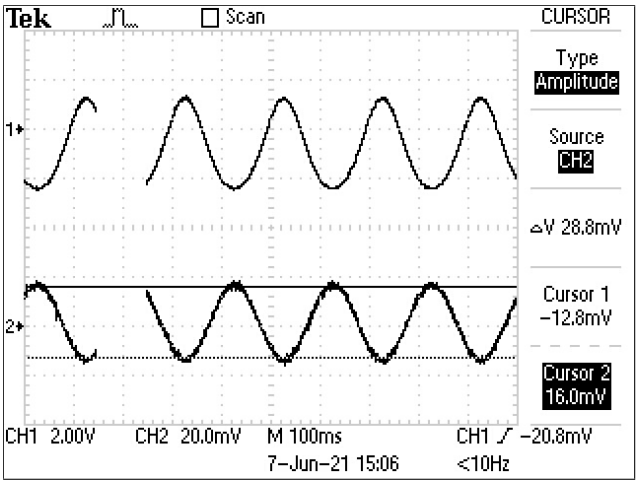


(b) Equivalent input noise and gain for $I_C = 10$ mA

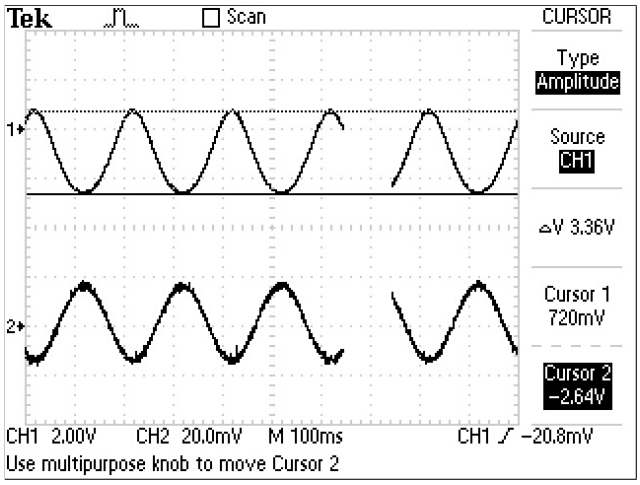
Figure B.3: Simulation results of ZXTN19100CFF transistor.

Appendix C

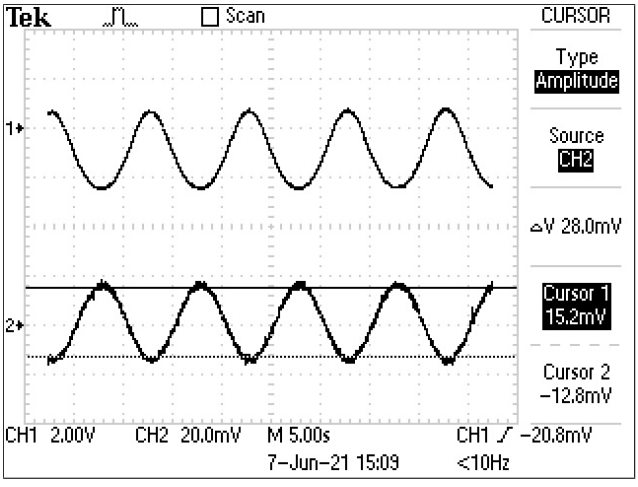
Common Emitter Amplifier Measurements



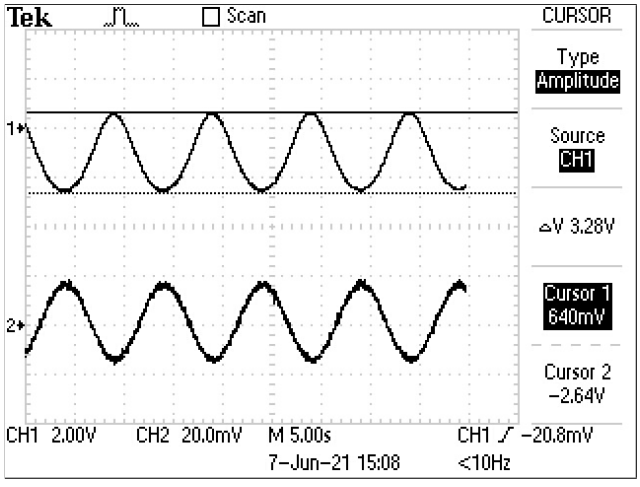
(a) Input at 5 Hz



(b) Output at 5 Hz

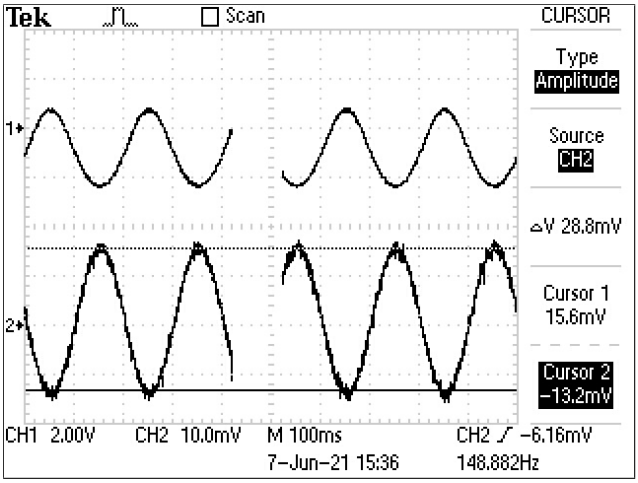


(c) Input at 100 mHz

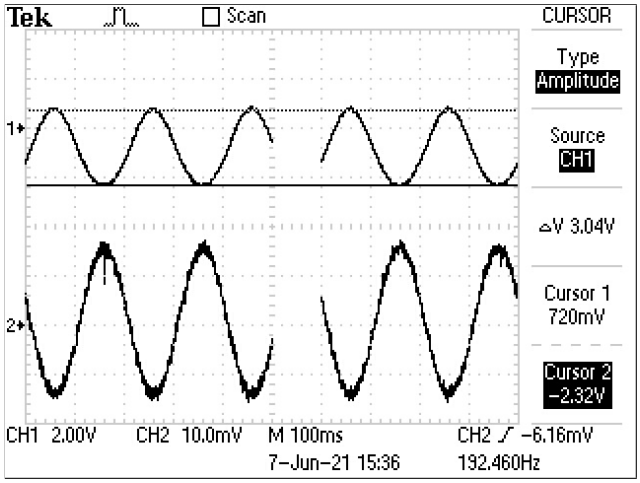


(d) Output at 100 mHz

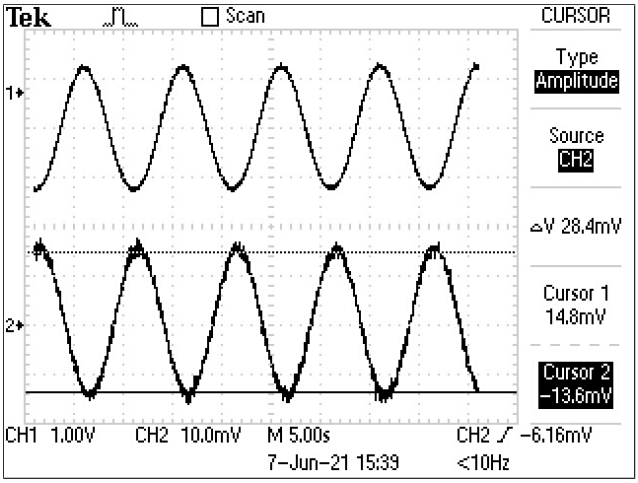
Figure C.1: Results of 2SA1312 transistor at 1 mA.



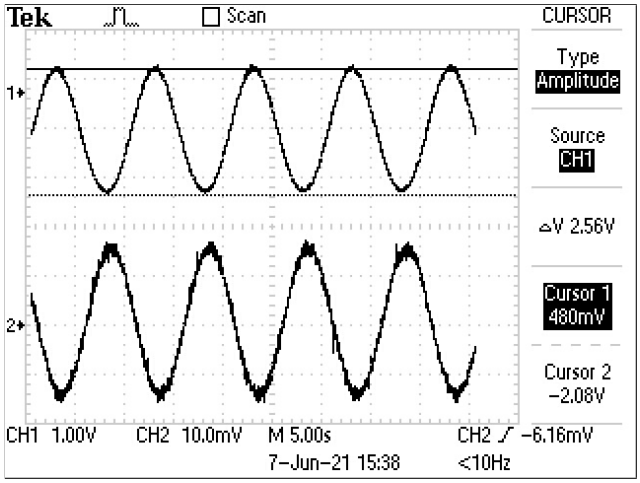
(a) Input at 5 Hz



(b) Output at 5 Hz

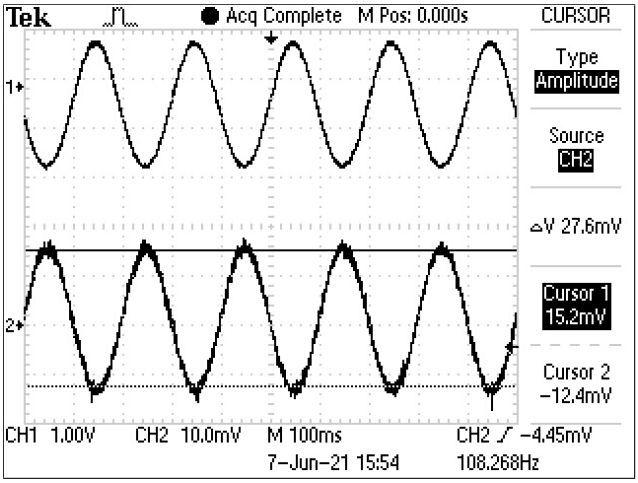


(c) Input at 100 mHz

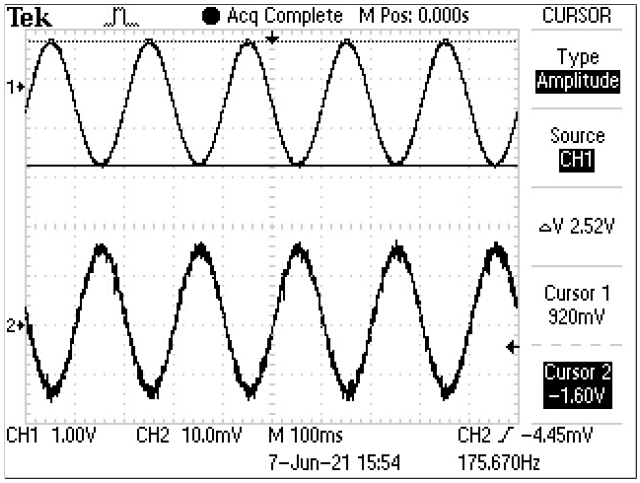


(d) Output at 100 mHz

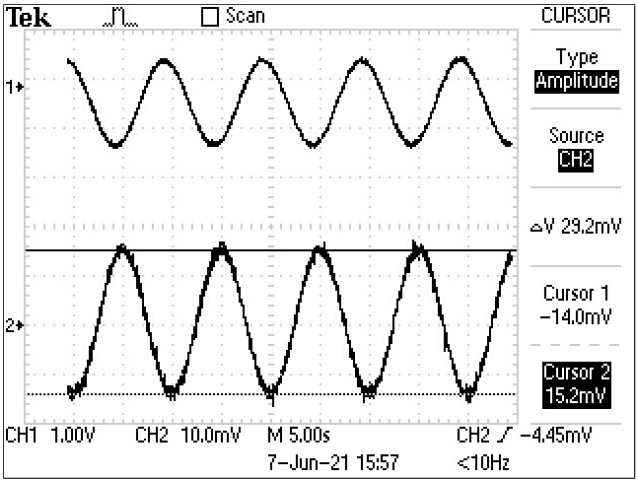
Figure C.2: Results of 2SA1312 transistor at 5 mA.



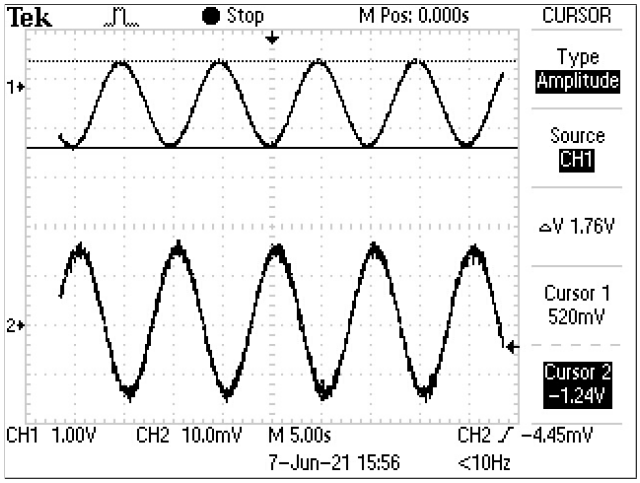
(a) Input at 5 Hz



(b) Output at 5 Hz

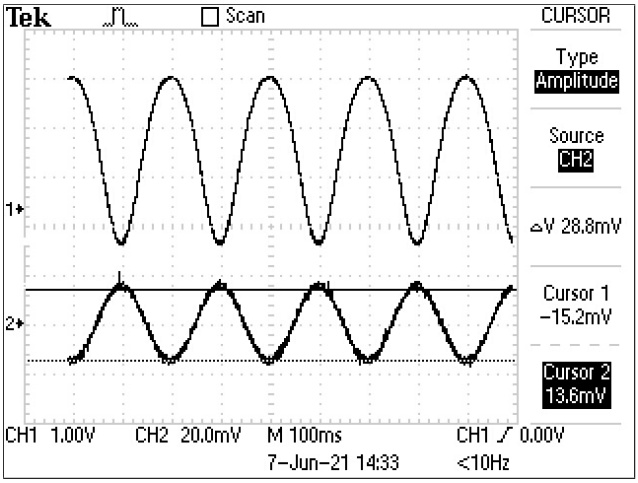


(c) Input at 100 mHz

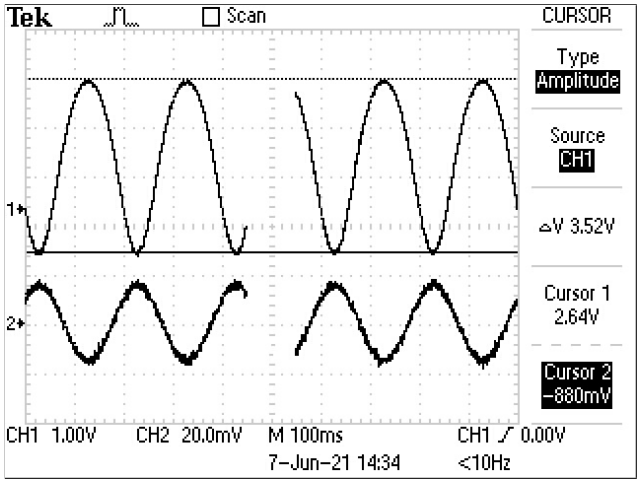


(d) Output at 100 mHz

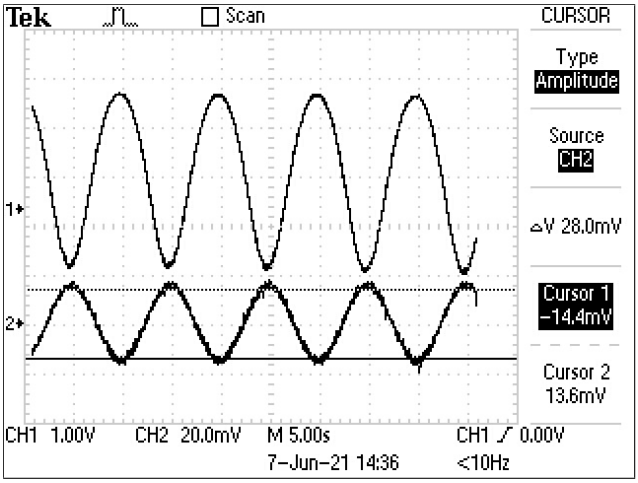
Figure C.3: Results of 2SA1312 transistor at 10 mA.



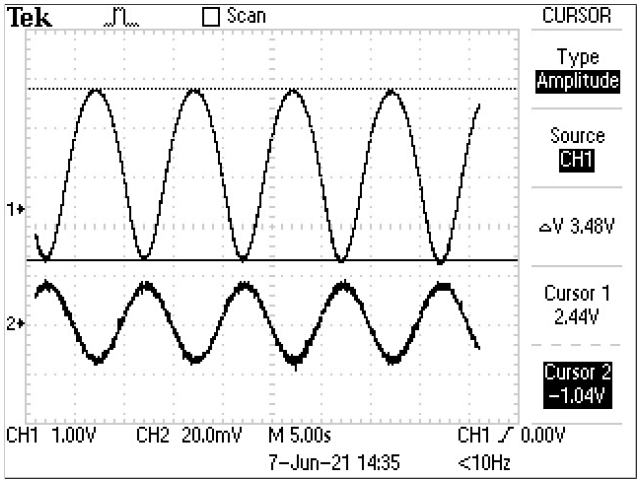
(a) Input at 5 Hz



(b) Output at 5 Hz

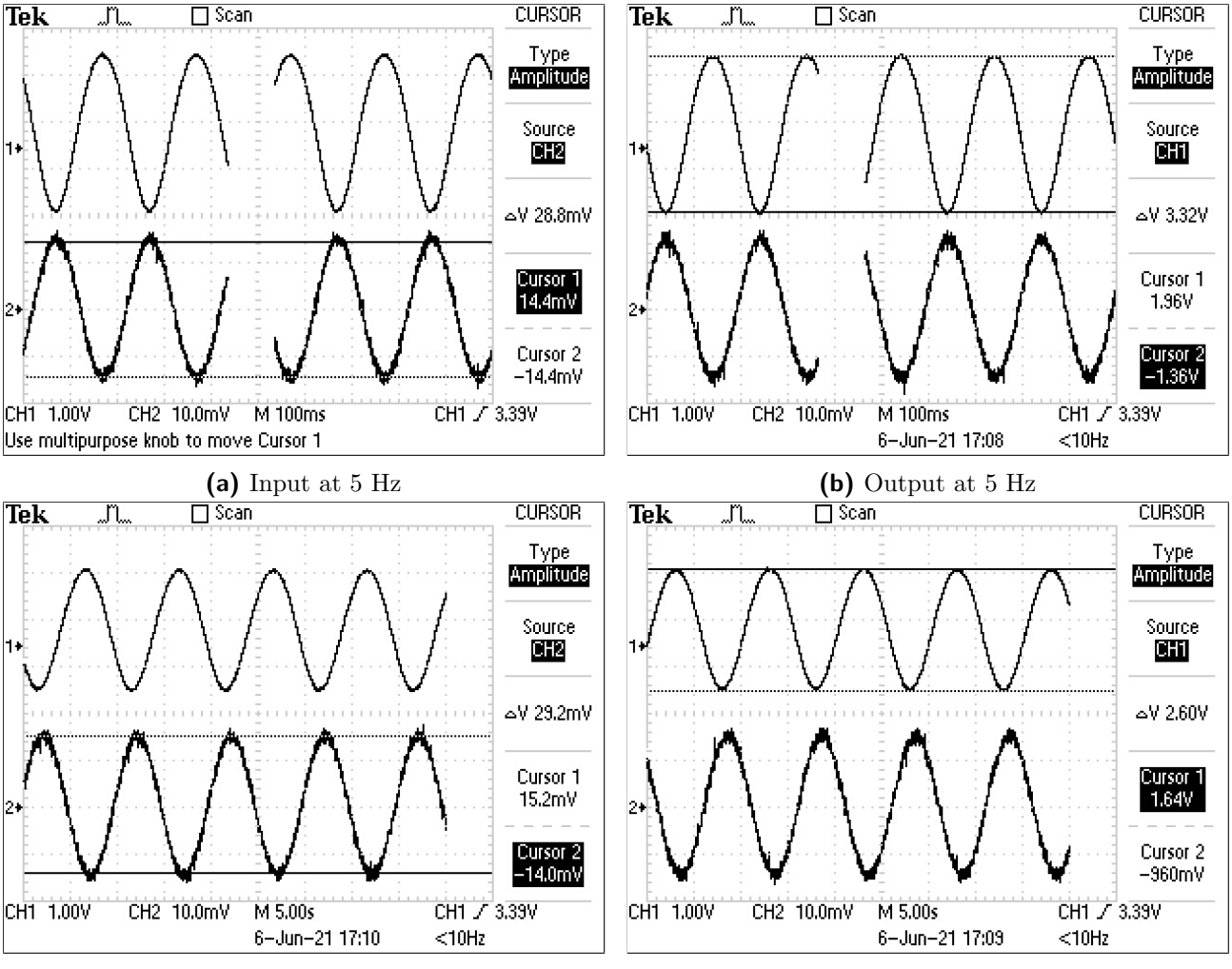


(c) Input at 100 mHz



(d) Output at 100 mHz

Figure C.4: Results of DSS20201L transistor at 1 mA.



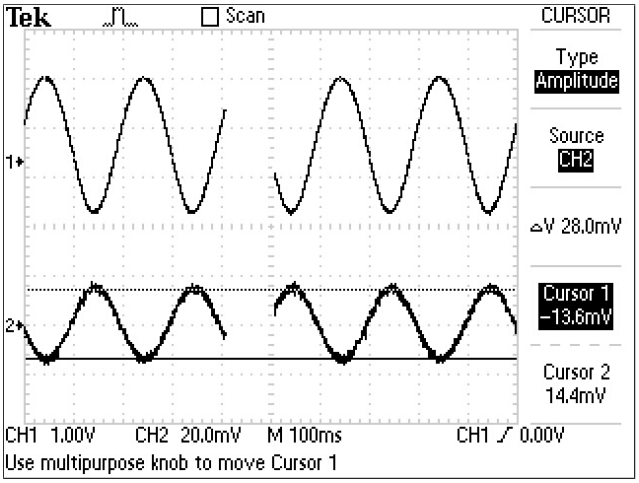
(a) Input at 5 Hz

(b) Output at 5 Hz

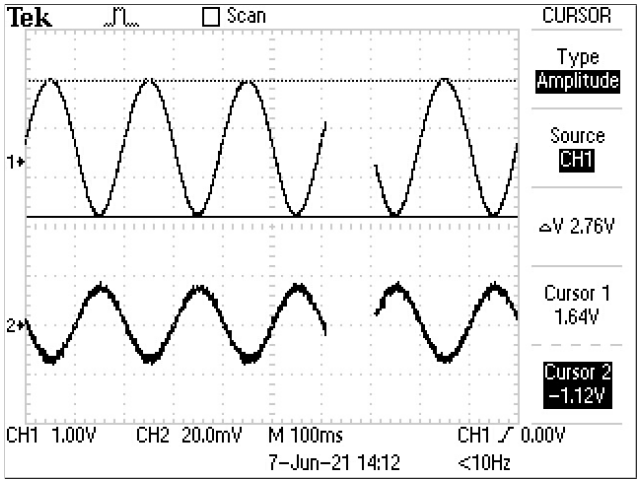
(c) Input at 100 mHz

(d) Output at 100 mHz

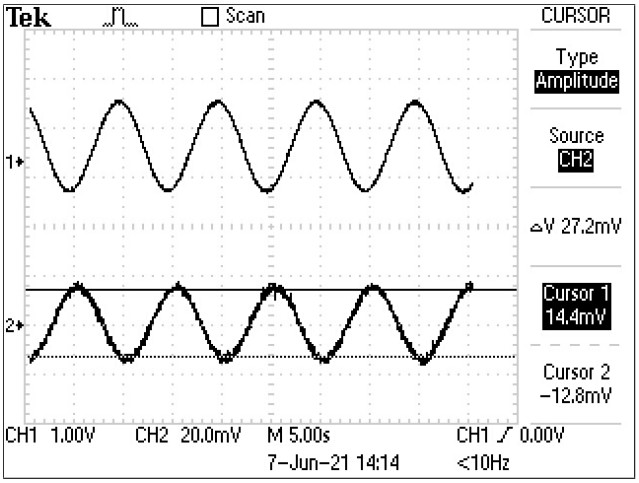
Figure C.5: Results of DSS20201L transistor at 5 mA.



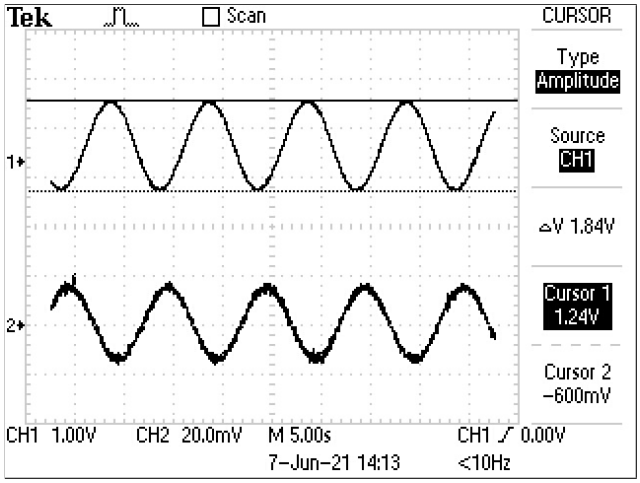
(a) Input at 5 Hz



(b) Output at 5 Hz

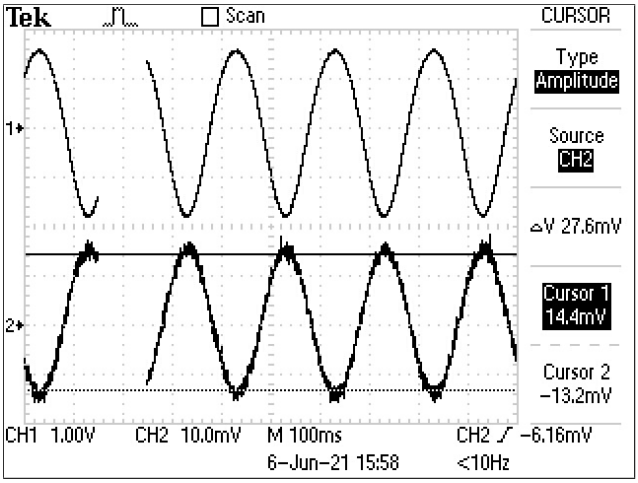


(c) Input at 100 mHz

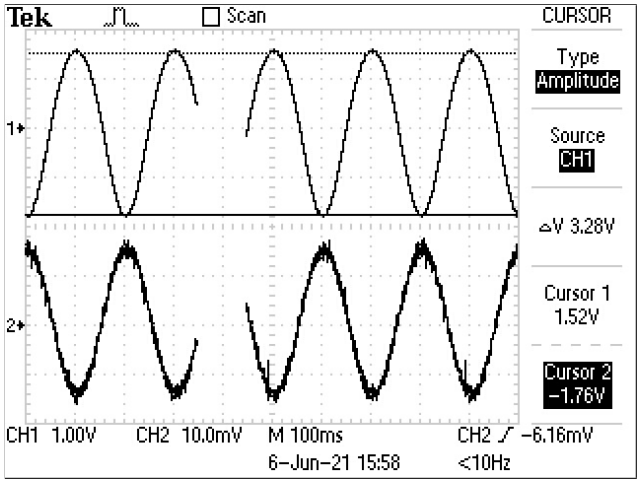


(d) Output at 100 mHz

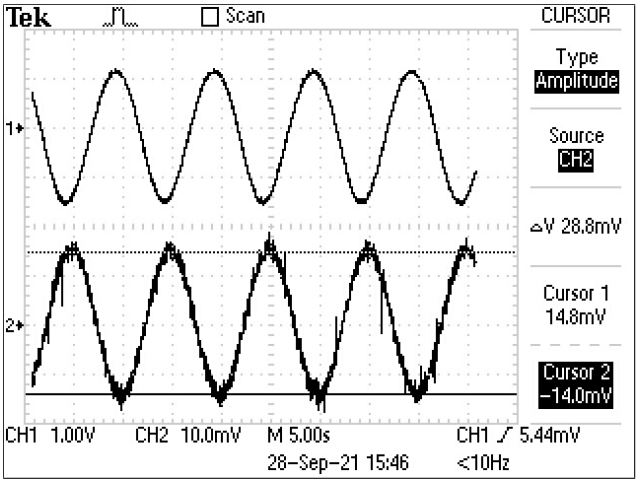
Figure C.6: Results of DSS20201L transistor at 10 mA.



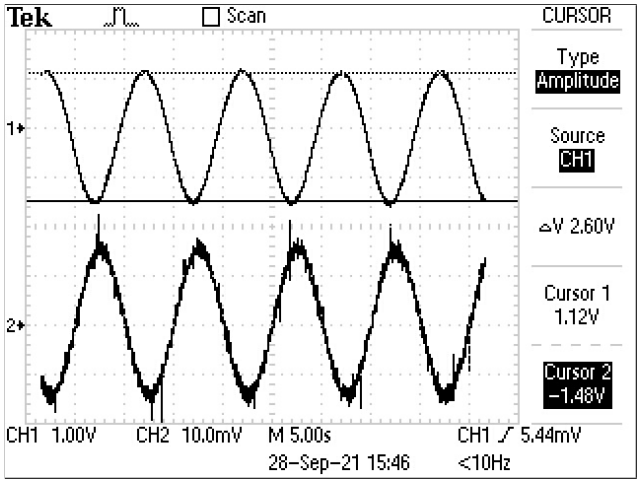
(a) Input at 5 Hz



(b) Output at 5 Hz

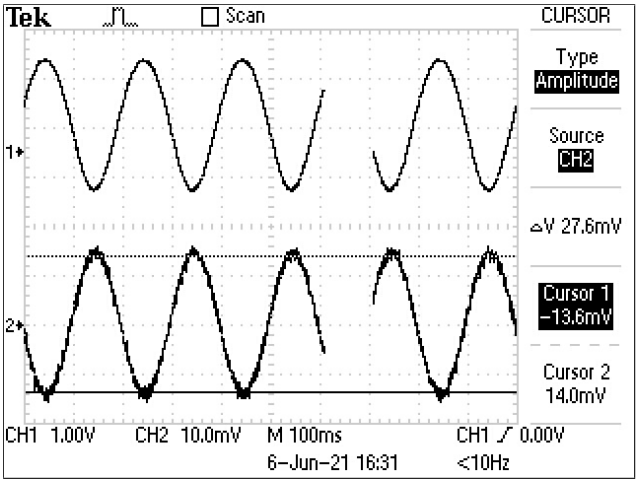


(c) Input at 100 mHz

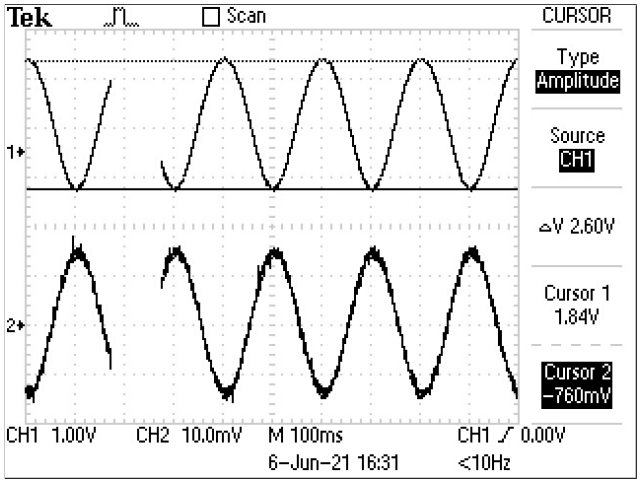


(d) Output at 100 mHz

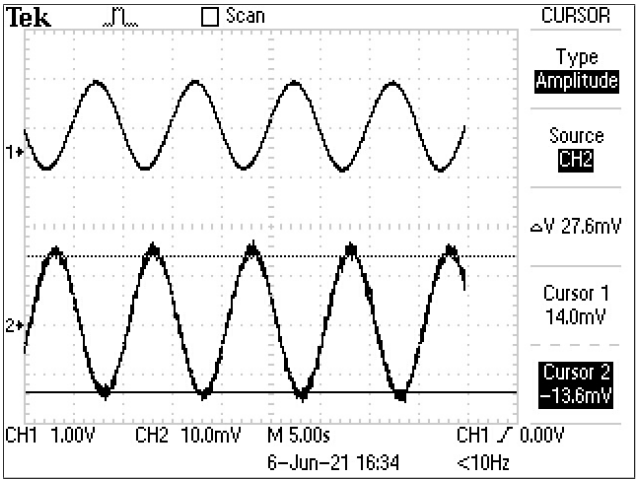
Figure C.7: Results of ZXTN19100CFF transistor at 5 mA.



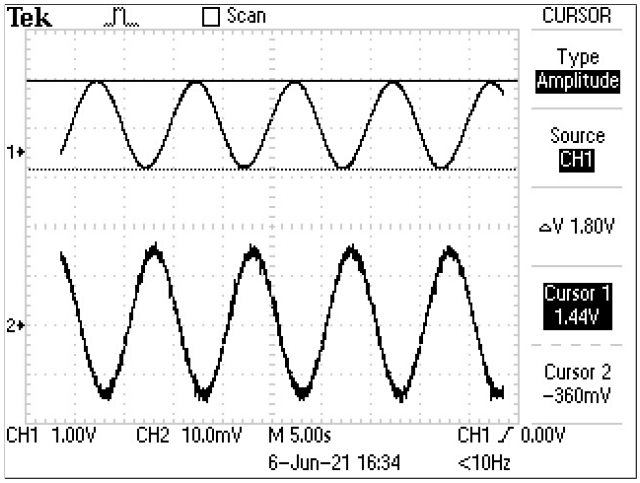
(a) Input at 5 Hz



(b) Output at 5 Hz



(c) Input at 100 mHz



(d) Output at 100 mHz

Figure C.8: Results of ZXTN19100CFF transistor at 10 mA.

Appendix D

Differential Amplifier Noise Calculation Comparison

Table D.1: Comparison of calculated and simulated noise for each noise source in a single stage differential amplifier with $I_{C1} = I_{C2} = 500\mu$A

	Noise Source	500 μA	
		Hand Calculation	**Spice Simulation**
Differential Amplifier	R_{B1}	519.498 n	518.266 n
	R_{B2}	519.498 n	518.266 n
	R_{C1}	25.033 n	24.193 n
	R_{C2}	25.033 n	24.194 n
	rx1	167.491 n	167.100 n
	rx2	167.491 n	167.100 n
	sic1	232.005 n	234.530 n
	sic2	232.028 n	234.254 n
	sib1/fib1	28.180 n	29.892 n
	sib2/fib2	28.180 n	29.893 n
Current Source	R_1	1.251 p	1.198 p
	rcx1	16.751 p	15.991 p
	rcx2	16.798 p	16.038 p
	sicc1	16.775 p	15.966 p
	sicc2	16.889 p	15.862 p
	sibc1/fibc1	0.375 p	0.369 p
	sibc2/fibc2	1.127 p	1.140 p
Instrumentation Amplifier	All R_A	1.287 n	1.288 n
	R_{GAIN}	1.820 n	1.821 n
	En1	2.400 n	NA
	En2	2.400 n	NA
	En3	2.400 n	NA
	Enf1	6.325 n	NA
	Enf2	6.325 n	NA
	Enf3	6.325 n	NA
	In1	34.059 n	NA

	In2	34.056 n	NA
	In3	180.000 p	NA
	Inf1	718.035 n	NA
	Inf2	717.964 n	NA
	Inf3	75.894 p	NA
TOTAL FLATBAND NOISE		**841.9 nV/$\sqrt{\text{Hz}}$**	**840.1 nV/$\sqrt{\text{Hz}}$**
TOTAL FLICKER NOISE		**1016.0 nV/$\sqrt{\text{Hz}}$**	**NA**

Table D.2: Comparison of calculated and simulated noise for each noise source in a single stage differential amplifier with $I_{C1} = I_{C2} = 1\text{mA}$

	Noise Source	**1 mA**	
		Hand Calculation	**Spice Simulation**
Differential Amplifier	R_{B1}	524.254 n	518.378 n
	R_{B2}	524.254 n	518.378 n
	R_{C1}	17.850 n	17.244 n
	R_{C2}	17.851 n	17.245 n
	rx1	168.982 n	167.172 n
	rx2	168.982 n	167.172 n
	sic1	166.741 n	167.194 n
	sic2	166.757n	167.195 n
	sib1/fib1	40.208 n	42.341 n
	sib2/fib2	40.208 n	42.342 n
Current Source	R_1	0.899 p	0.860 p
	rcx1	17.017 p	15.942 p
	rcx2	17.065 p	15.991 p
	sicc1	12.062 p	11.321 p
	sicc2	12.144 p	11.251 p
	sibc1/fibc1	0 p	0.002 p
	sibc2/fibc2	1.080 p	1.088 p
Instrumentation Amplifier	All R_A	1.287 n	1.288 n
	R_{GAIN}	1.820 n	1.821 n
	En1	2.400 n	NA
	En2	2.400 n	NA
	En3	2.400 n	NA
	Enf1	6.325 n	NA
	Enf2	6.325 n	NA
	Enf3	6.325 n	NA
	In1	17.318 n	NA
	In2	17.316 n	NA
	In3	180.000 p	NA
	Inf1	365.090 n	NA
	Inf2	365.053 n	NA
	Inf3	75.894 p	NA
TOTAL FLATBAND NOISE		**816.6 nV/$\sqrt{\text{Hz}}$**	**808.3 nV/$\sqrt{\text{Hz}}$**
TOTAL FLICKER NOISE		**519.5 nV/$\sqrt{\text{Hz}}$**	**NA**

Table D.3: Comparison of calculated and simulated noise for each noise source in a single stage differential amplifier with $I_{C1} = I_{C2} = 2\text{mA}$

	Noise Source	2 mA	
		Hand Calculation	**Spice Simulation**
Differential Amplifier	R_{B1}	532.444 n	518.368 n
	R_{B2}	532.444 n	518.368 n
	R_{C1}	12.817 n	12.370 n
	R_{C2}	12.818 n	12.370 n
	rx1	171.535 n	167.169 n
	rx2	171.535 n	167.169 n
	sic1	121.463 n	120.261 n
	sic2	121.475 n	120.261 n
	sib1/fib1	57.721 n	60.024 n
	sib2/fib2	57.721 n	60.025 n
Current Source	R_1	0.656 p	0.588 p
	rcx1	17.513 p	14.915 p
	rcx2	17.562 p	14.962 p
	sicc1	8.795 p	7.567 p
	sicc2	8.855 p	7.526 p
	sibc1/fibc1	0.392 p	0.350 p
	sibc2/fibc2	1.181 p	1.097 p
Instrumentation Amplifier	All R_A	1.287 n	1.288 n
	R_{GAIN}	1.820 n	1.821 n
	En1	2.400 n	NA
	En2	2.400 n	NA
	En3	2.400 n	NA
	Enf1	6.325 n	NA
	Enf2	6.325 n	NA
	Enf3	6.325 n	NA
	In1	8.929 n	NA
	In2	8.928 n	NA
	In3	180.000 p	NA
	Inf1	188.238 n	NA
	Inf2	188.219 n	NA
	Inf3	75.894 p	NA
TOTAL FLATBAND NOISE		**814.0 nV/$\sqrt{\text{Hz}}$**	**793.6 nV/$\sqrt{\text{Hz}}$**
TOTAL FLICKER NOISE		**278.6 nV/$\sqrt{\text{Hz}}$**	**NA**

Table D.4: Comparison of calculated and simulated noise for each noise source in a multistage stage differential amplifier with $I_{C1} = I_{C2} = I_{C3} = I_{C4} = 500\mu\text{A}$. The noise is calculated for the case where all assumptions are used and for the case where few assumptions are used.

	Noise Source	500 μA		
		All Assumptions	**Few Assumptions**	**Spice Simulation**
Differential Amplifier 1	R_{B1}	897.207 n	929.661 n	930.112 n
	R_{B2}	897.207 n	929.661 n	930.112 n

	R_{C1}	454.517 n	477.372 n	457.187 n
	R_{C2}	454.537 n	477.475 n	457.209 n
	rx1	1.446 μ	1.498 μ	1.500 μ
	rx2	1.446 μ	1.498 μ	1.500 μ
	sic1	2.052 μ	2.196 μ	2.091 μ
	sic2	2.052 μ	2.196 μ	2.091 μ
	sib1/fib1	31.738 n	34.403 n	35.009 n
	sib2/fib2	31.738 n	34.403 n	35.019 n
Differential Amplifier 2	R_{C3}	11.740 n	11.734 n	11.733 n
	R_{C4}	11.740 n	11.735 n	11.734 n
	rx3	35.908 n	37.720 n	36.160 n
	rx4	35.908 n	37.726 n	36.160 n
	sic3	53.006 n	54.746 n	54.353 n
	sic4	53.012 n	54.650 n	54.437 n
	sib3/fib3	92.943 n	105.091 n	100.024 n
	sib4/fib4	92.952 n	104.918 n	99.834 n
Current Source 1	R_1	10.382 p	10.915 p	10.949 p
	rcx1	138.976 p	147.803 p	146.163 p
	rcx2	139.364 p	148.211 p	146.600 p
	sicc1	139.173 p	147.157 p	145.938 p
	sicc2	140.119 p	146.174 p	144.992 p
	sibc1/fibc1	3.109 p	3.392 p	3.375 p
	sibc2/fibc2	9.348 p	10.356 p	10.421 p
Current Source 2	R_2	0.254 p	9.758 p	9.695 p
	rcx3	3.406 p	132.144 p	129.428 p
	rcx4	3.415 p	132.509 p	129.815 p
	sicc3	3.411 p	131.566 p	129.227 p
	sicc4	3.434 p	128.950 p	126.664 p
	sibc3/fibc3	0.076 p	3.032 p	2.987 p
	sibc4/fibc4	0.229 p	9.257 p	9.226 p
Instrumentation Amplifier	All R_A	1.287 n	1.287 n	1.288 n
	R_{GAIN}	1.820 n	1.820 n	1.821 n
	En1	2.400 n	2.400 n	NA
	En2	2.400 n	2.400 n	NA
	En3	2.400 n	2.400 n	NA
	Enf1	6.325 n	6.325 n	NA
	Enf2	6.325 n	6.325 n	NA
	Enf3	6.325 n	6.325 n	NA
	In1	7.597 n	7.597 n	NA
	In2	7.596 n	7.596 n	NA
	In3	180.000 p	180.000 p	NA
	Inf1	160.154 n	160.154 n	NA
	Inf2	160.138 n	160.138 n	NA
	Inf3	75.895 p	75.895 p	NA
TOTAL FLATBAND NOISE		**3.828 μV/$\sqrt{\text{Hz}}$**	**4.044 μV/$\sqrt{\text{Hz}}$**	**3.927 μV/$\sqrt{\text{Hz}}$**
TOTAL FLICKER NOISE		**265.9 nV/$\sqrt{\text{Hz}}$**	**275.4 nV/$\sqrt{\text{Hz}}$**	**NA**

Table D.5: Comparison of calculated and simulated noise for each noise source in a multistage stage differential amplifier with $I_{C1} = I_{C2} = I_{C3} = I_{C4} = 1$ mA. The noise is calculated for the case where all assumptions are used and for the case where few assumptions are used.

	Noise Source	1 mA		
		All Assumptions	Few Assumptions	Spice Simulation
Differential Amplifier 1	R_{B1}	921.135 n	934.274 n	934.728 n
	R_{B2}	921.135 n	934.274 n	934.728 n
	R_{C1}	327.869 n	340.594 n	326.161 n
	R_{C2}	327.883 n	340.669 n	326.177 n
	rx1	1.484 μ	1.505 μ	1.507 μ
	rx2	1.484 μ	1.505 μ	1.507 μ
	sic1	1.491 μ	1.576 μ	1.491 μ
	sic2	1.491 μ	1.576 μ	1.491 μ
	sib1/fib1	46.065 n	48.930 n	49.814 n
	sib2/fib2	46.065 n	48.930 n	49.821 n
Differential Amplifier 2	R_{C3}	8.359 n	8.335 n	8.355 n
	R_{C4}	8.360 n	8.356 n	8.355 n
	rx3	36.368 n	37.784 n	36.228 n
	rx4	36.368 n	37.790 n	36.228 n
	sic3	38.010 n	39.203 n	38.708 n
	sic4	38.014 n	39.134 n	38.768 n
	sib3/fib3	67.910 n	76.017 n	72.374 n
	sib4/fib4	67.917 n	75.892 n	72.237 n
Current Source 1	R_1	7.539 p	7.995 p	7.858 p
	rcx1	142.575 p	152.639 p	145.698 p
	rcx2	142.974 p	153.062 p	146.142 p
	sicc1	101.059 p	107.684 p	103.454 p
	sicc2	101.747 p	106.994 p	102.823 p
	sibc1/fibc1	0 p	0.048 p	0.015 p
	sibc2/fibc2	9.052 p	10.145 p	9.947 p
Current Source 2	R_2	0.182 p	6.996 p	6.889 p
	rcx3	3.447 p	133.573 p	127.731 p
	rcx4	3.456 p	133.943 p	128.118 p
	sicc3	2.443 p	94.234 p	90.698 p
	sicc4	2.460 p	92.400 p	88.949 p
	sibc3/fibc3	0 p	0.042 p	0.013 p
	sibc4/fibc4	0.218 p	8.875 p	8.714 p
Instrumentation Amplifier	All R_A	1.287 n	1.287 n	1.288 n
	R_{GAIN}	1.820 n	1.820 n	1.821 n
	En1	2.400 n	2.400 n	NA
	En2	2.400 n	2.400 n	NA
	En3	2.400 n	2.400 n	NA
	Enf1	6.325 n	6.325 n	NA
	Enf2	6.325 n	6.325 n	NA
	Enf3	6.325 n	6.325 n	NA
	In1	3.853 n	3.853 n	NA

	In2	3.852 n	3.852 n	NA
	In3	180.000 p	180.000 p	NA
	Inf1	81.215 n	81.215 n	NA
	Inf2	81.207 n	81.207 n	NA
	Inf3	75.895 p	75.895 p	NA
TOTAL FLATBAND NOISE		**3.284 μV/$\sqrt{\text{Hz}}$**	**3.391 μV/$\sqrt{\text{Hz}}$**	**3.312 μV/$\sqrt{\text{Hz}}$**
TOTAL FLICKER NOISE		**163.6 nV/$\sqrt{\text{Hz}}$**	**172.2 nV/$\sqrt{\text{Hz}}$**	**NA**

Table D.6: Comparison of calculated and simulated noise for each noise source in a multistage stage differential amplifier with $I_{C1} = I_{C2} = I_{C3} = I_{C4} = 2$ mA. The noise is calculated for the case where all assumptions are used and for the case where few assumptions are used.

	Noise Source	**2 mA**		
		All Assumptions	**Few Assumptions**	**Spice Simulation**
Differential Amplifier 1	R_{B1}	969.791 n	947.025 n	947.485 n
	R_{B2}	969.791 n	947.025 n	947.485 n
	R_{C1}	241.066 n	245.560 n	235.125 n
	R_{C2}	241.077 n	245.615 n	235.136 n
	rx1	1.562 μ	1.525 μ	1.528 μ
	rx2	1.562 μ	1.525 μ	1.528 μ
	sic1	1.111 μ	1.150 μ	1.076 μ
	sic2	1.112 μ	1.150 μ	10.76 μ
	sib1/fib1	68.539 n	70.221 n	71.547 n
	sib2/fib2	68.539 n	70.221 n	71.551 n
Differential Amplifier 2	R_{C3}	5.992 n	5.989 n	5.989 n
	R_{C4}	5.992 n	5.990 n	5.990 n
	rx3	37.284 n	37.979 n	36.431 n
	rx4	37.284 n	37.986 n	36.431 n
	sic3	27.625 n	28.443 n	27.784 n
	sic4	27.628 n	28.393 n	27.826 n
	sib3/fib3	51.184 n	56.265 n	53.604 n
	sib4/fib4	51.188 n	56.171 n	53.501 n
Current Source 1	R_1	5.615 p	5.536 p	5.736 p
	rcx1	149.881 p	148.839 p	145.446 p
	rcx2	150.301 p	149.253 p	145.902 p
	sicc1	75.271 p	74.489 p	73.790 p
	sicc2	75.783 p	74.045 p	73.386 p
	sibc1/fibc1	3.353 p	3.543 p	3.416 p
	sibc2/fibc2	10.104 p	10.569 p	10.699 p
Current Source 2	R_2	0.132 p	5.086 p	4.927 p
	rcx3	3.527 p	136.729 p	124.937 p
	rcx4	3.537 p	137.110 p	125.330 p
	sicc3	1.771 p	68.429 p	63.836 p
	sicc4	1.784 p	67.150 p	62.224 p
	sibc3/fibc3	0.079 p	3.255 p	2.934 p
	sibc4/fibc4	0.238 p	9.703 p	9.184 p

Instrumentation Amplifier	All R_A	1.287 n	1.287 n	1.288 n
	R_{GAIN}	1.820 n	1.820 n	1.821 n
	En1	2.400 n	2.400 n	NA
	En2	2.400 n	2.400 n	NA
	En3	2.400 n	2.400 n	NA
	Enf1	6.325 n	6.325 n	NA
	Enf2	6.325 n	6.325 n	NA
	Enf3	6.325 n	6.325 n	NA
	In1	1.980 n	1.980 n	NA
	In2	1.980 n	1.980 n	NA
	In3	180.000 p	180.000 p	NA
	Inf1	41.746 n	41.746 n	NA
	Inf2	41.742 n	41.742 n	NA
	Inf3	75.895 p	75.895 p	NA
TOTAL FLATBAND NOISE		**7.284 μV/$\sqrt{\text{Hz}}$**	**7.128 μV/$\sqrt{\text{Hz}}$**	**7.116 μV/$\sqrt{\text{Hz}}$**
TOTAL FLICKER NOISE		**729.1 nV/$\sqrt{\text{Hz}}$**	**745.7 nV/$\sqrt{\text{Hz}}$**	**NA**

Appendix E

Simulation Schematic

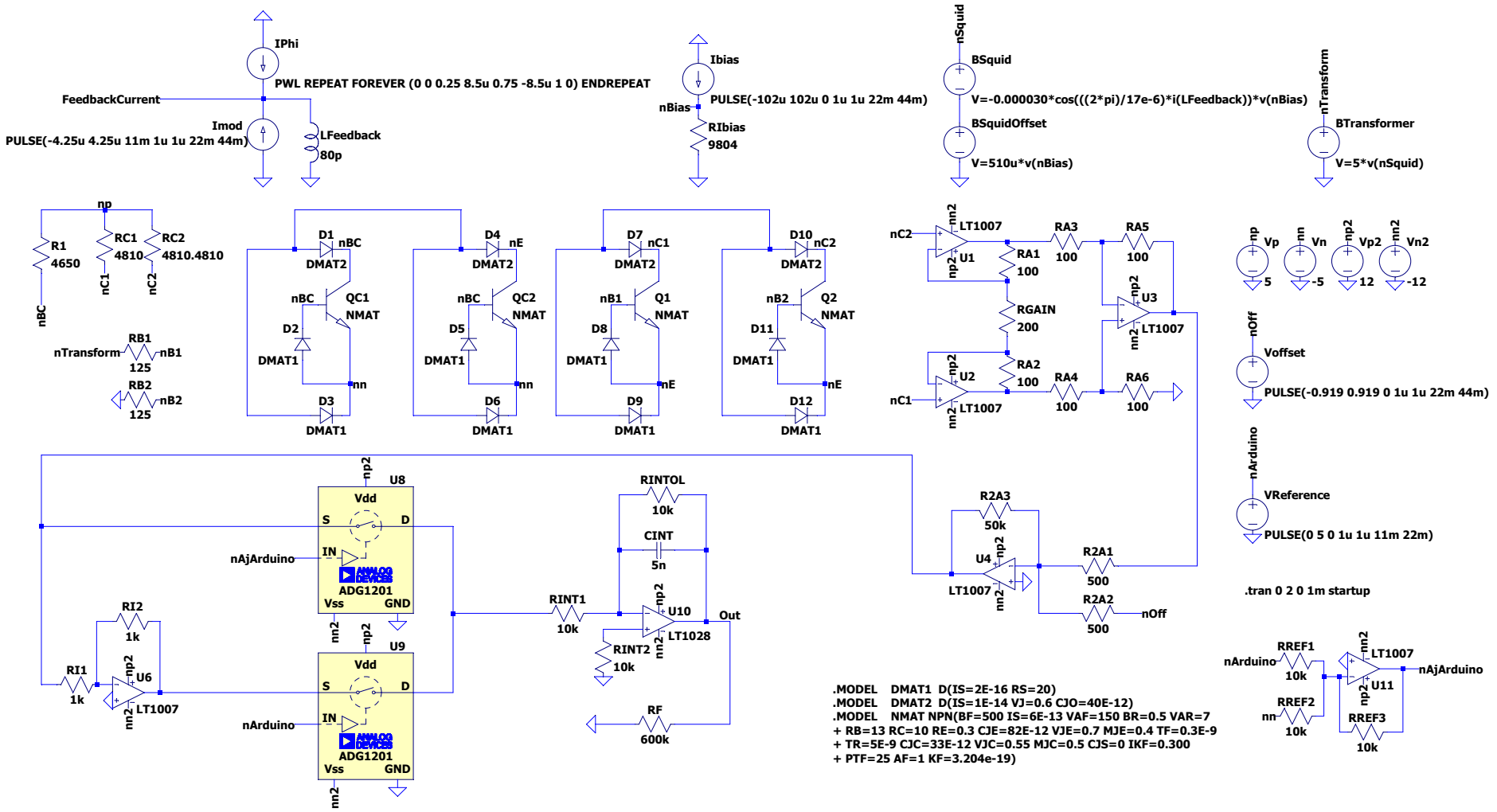


Figure E.1: LTspice schematic of the Flux-Locked-Loop